14" Discrete Block Diagram

PCB Stackups

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

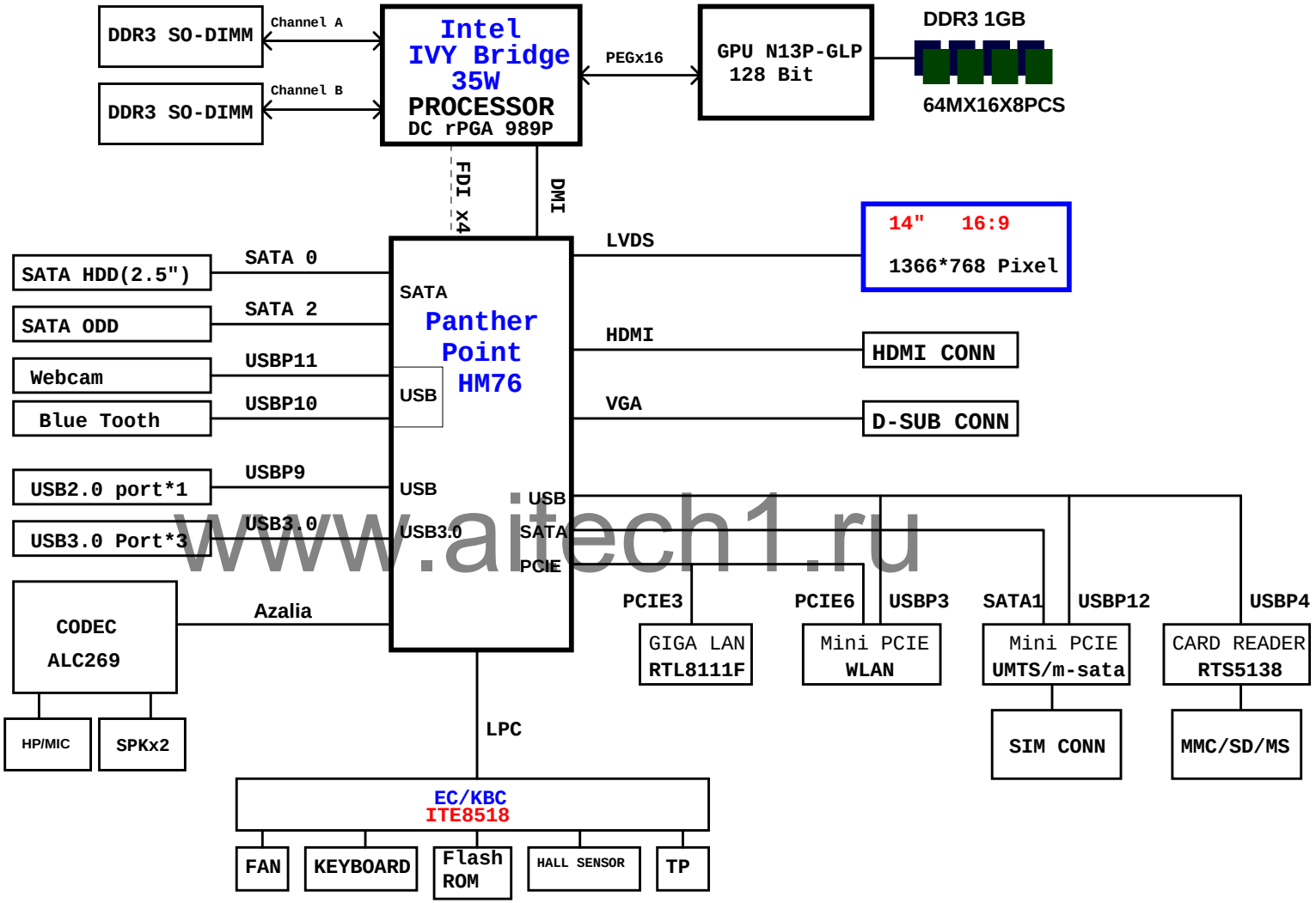

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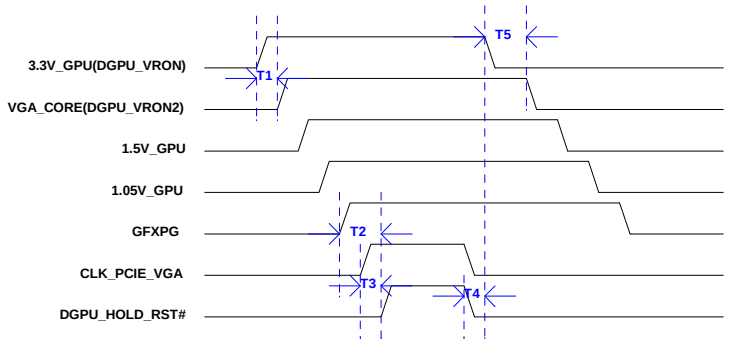
Table of Contents

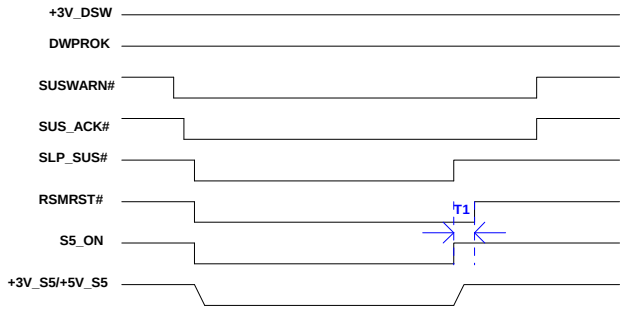
POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0~S5
3V_RTC	+3.0V~+3.3V		S0~G3
3V_S0	+3.3V	S0_ON1	S0
3V_S5	+3.3V	EC	S0~S5
3V_AUX	+3.3V	AC/DC Insert enable	AWLAYS
5V_S0	+5V	S0_ON1	S0
5V_S3	+5V	S3_ON	S0~S3
5V_S5	+5V	EC	S0~S5
5V_AUX	+5V	AC/DC Insert enable	AWLAYS
1.8V_S0	+1.8V	S0_ON2	S0
1.5V_S0	+1.5V	S0_ON2	S0
1.5V_S3	+1.5V	S3_ON	S0~S3
1.05V_S0	+1.05V	S0_ON2	S0
VCCSA	By VID	S0_ON2	S0
CPU_CORE	By VID	VR_ON	S0
VCC_AXG	By VID	VR_ON	S0
3V_LAN	+3.3V	LAN_ON	S0~S5(By WOL)
3V_GPU	+3.3V	DGPU_VRON	Optimus
1.5V_GPU	+1.5V	DGFX_VR_PWRGD	Optimus
1.05V_GPU	+1.05V	DGFX_VR_PWRGD	Optimus
VGA_CORE	By VID	DGPU_VRON1	Optimus

N13P-LP Power ON/OFF Sequence



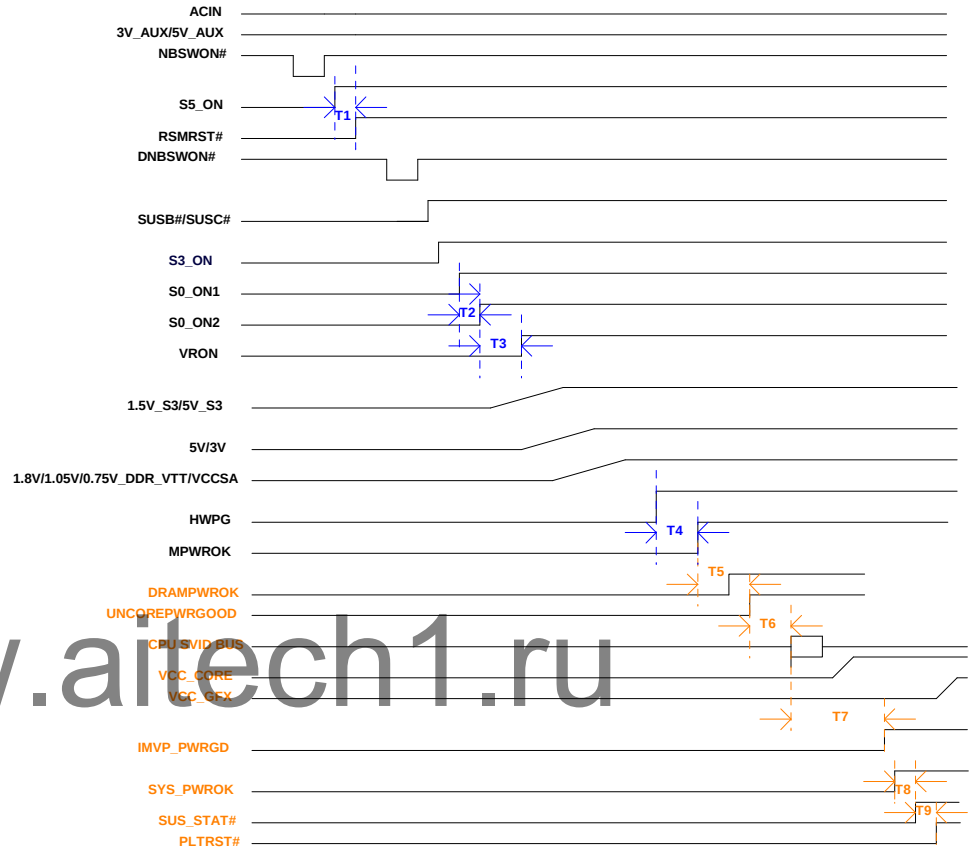
BIOS/ EC control:
T1:DGPU_VRON to DGPU_VRON2 = 500us
T2:GFXPG to DGPU_HOLD_RST# = 5ms
T3:CLK_PCIE_VGA to DGPU_HOLD_RST# >100us(Spec)
T4:DGPU_HOLD_RST# to DGPU_VRON = 5ms
Note: Clock must be shutdown before 3.3V_GPU
T5:DGPU_VRON to DGPU_VRON2 = 500us

Deep S4/S5 off-on Sequence



Deep S4/S5 Sequence
T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)

System Power-ON Sequence



System Power Sequence

EC Control:
T1: S5_ON TO RSMRST# = 20ms (spec:mini 10ms)
T2: S0_ON1 TO S0_ON2 = 500us
T3: S0_ON2 TO VRON = 10ms
T4: HWPG TO MPWROK = 110ms (spec:mini 99ms)
Note:HWPG NEED TO BE HIGH at that time

System:
T5: MPWROK to UNCOREPWRGOOD =2ms(Min)
T6: UNCOREPWRGOOD to SVID Packet =500us(Max)
T7: SVID Packet to IMVP_PWRGD =5ms(Max)
T8: SYS_PWROK to SUS_STAT# =1ms(Min)
T9:SUS_STAT# to PLTRST# =60us(Min)

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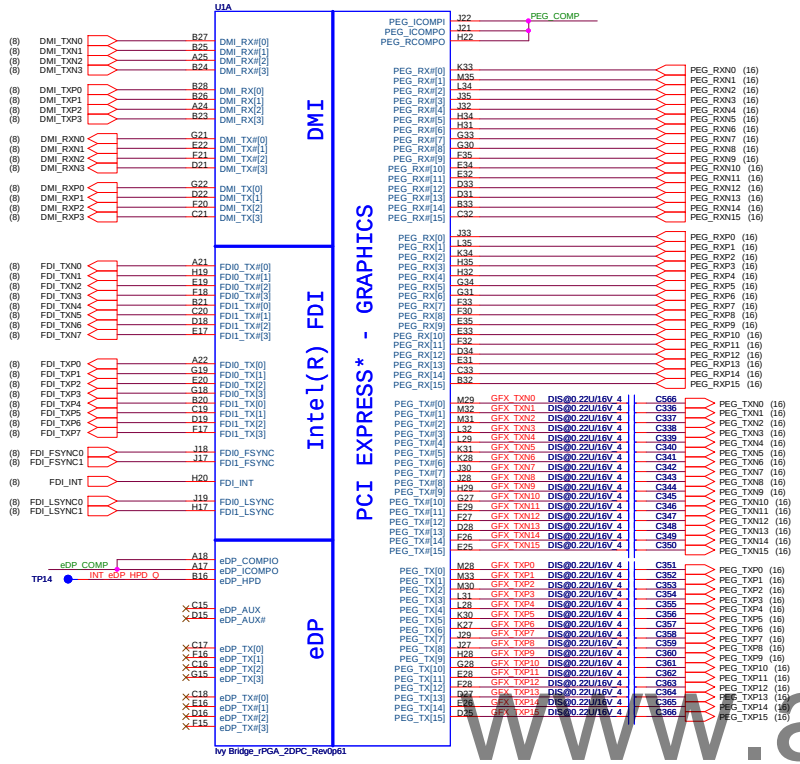
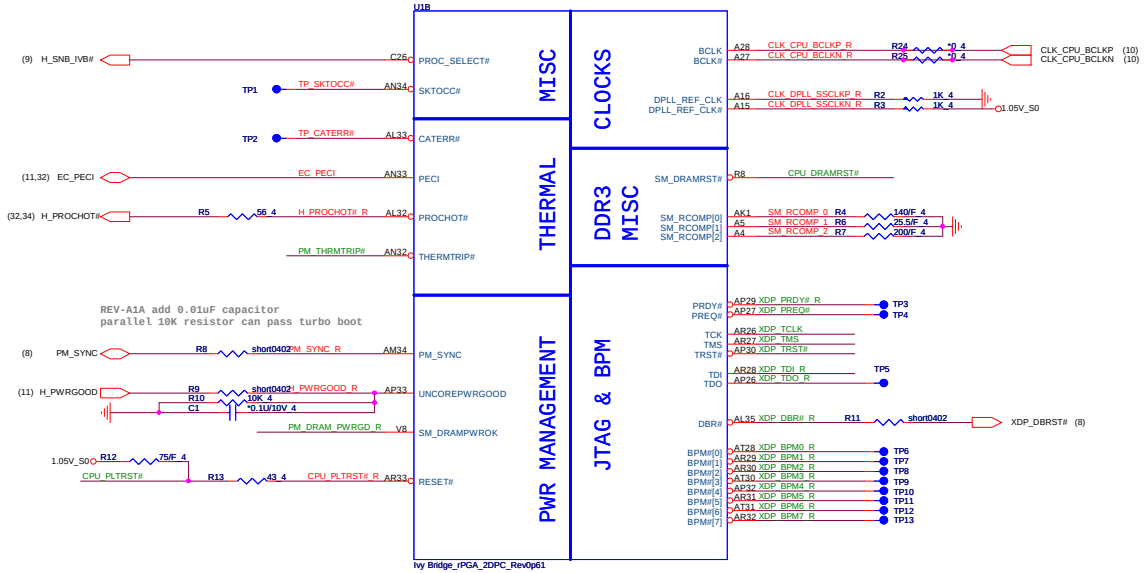
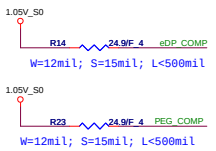
Ivy Bridge Processor (DMI,PEG,FDI)



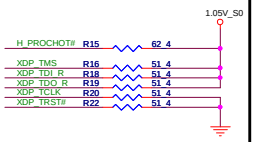
Ivy Bridge Processor (CLK,MISC,JTAG)



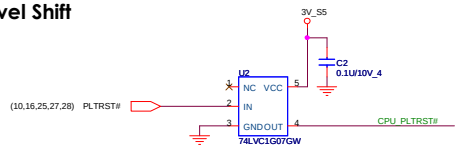
DP & PEG Compensation



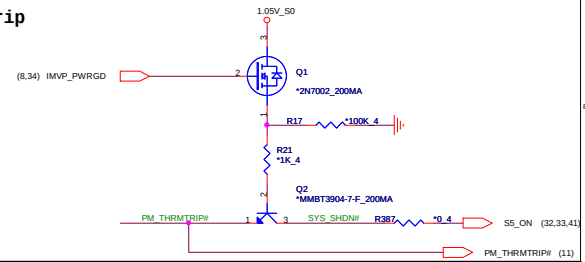
Processor pull-up



Level Shift



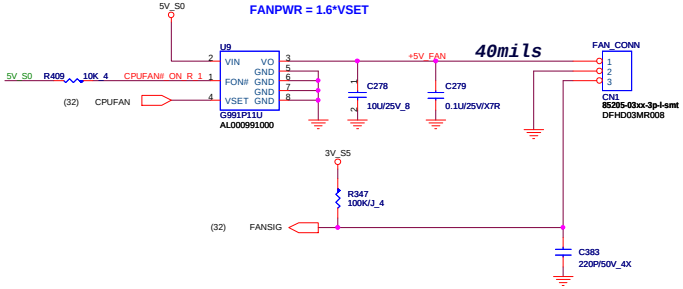
Thermal Trip



FAN Control-->For one FAN solution

VSET >= 1V, Enable

FANPWR = 1.6*VSET



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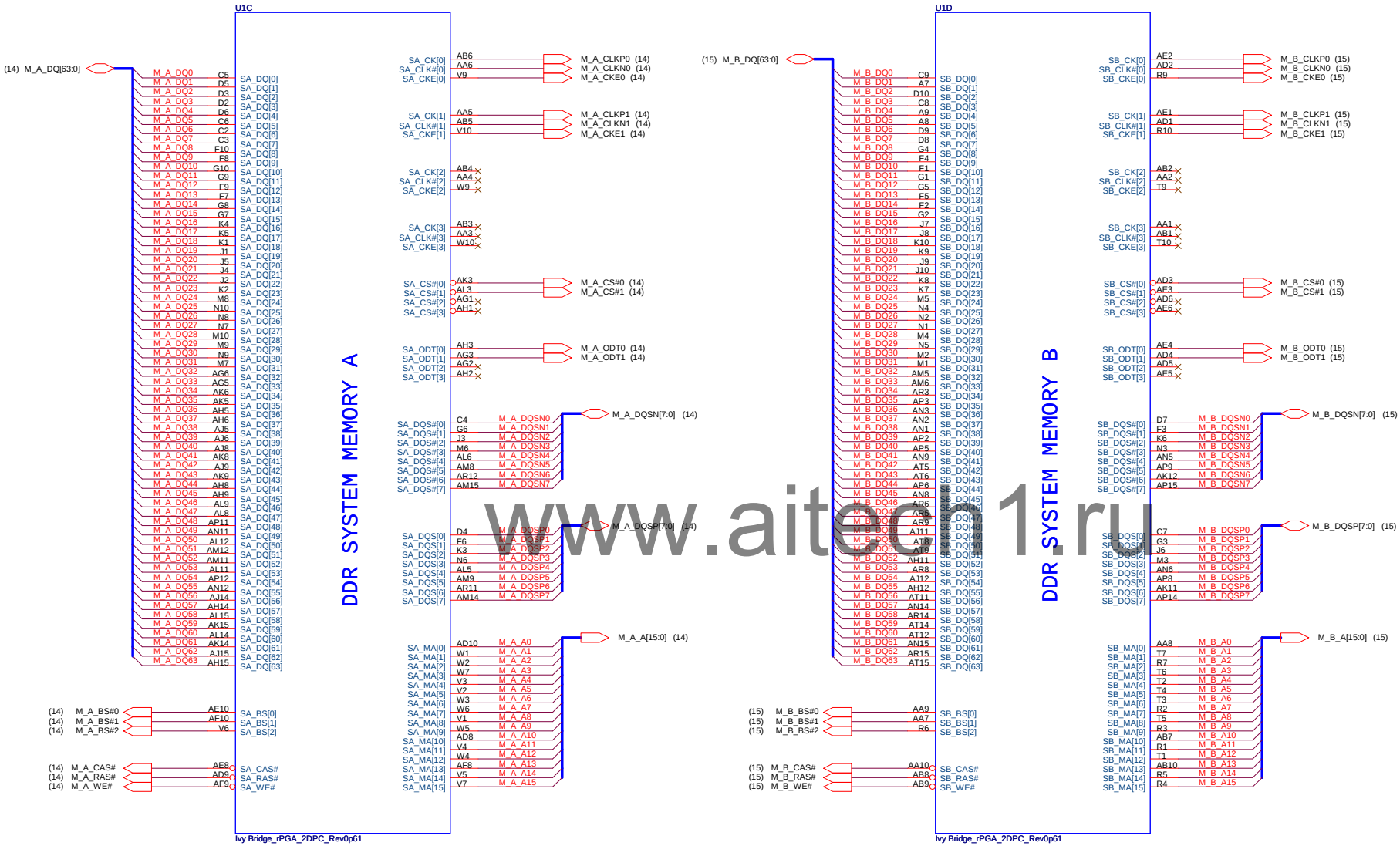
Ivy Bridge Processor (DDR3)

05



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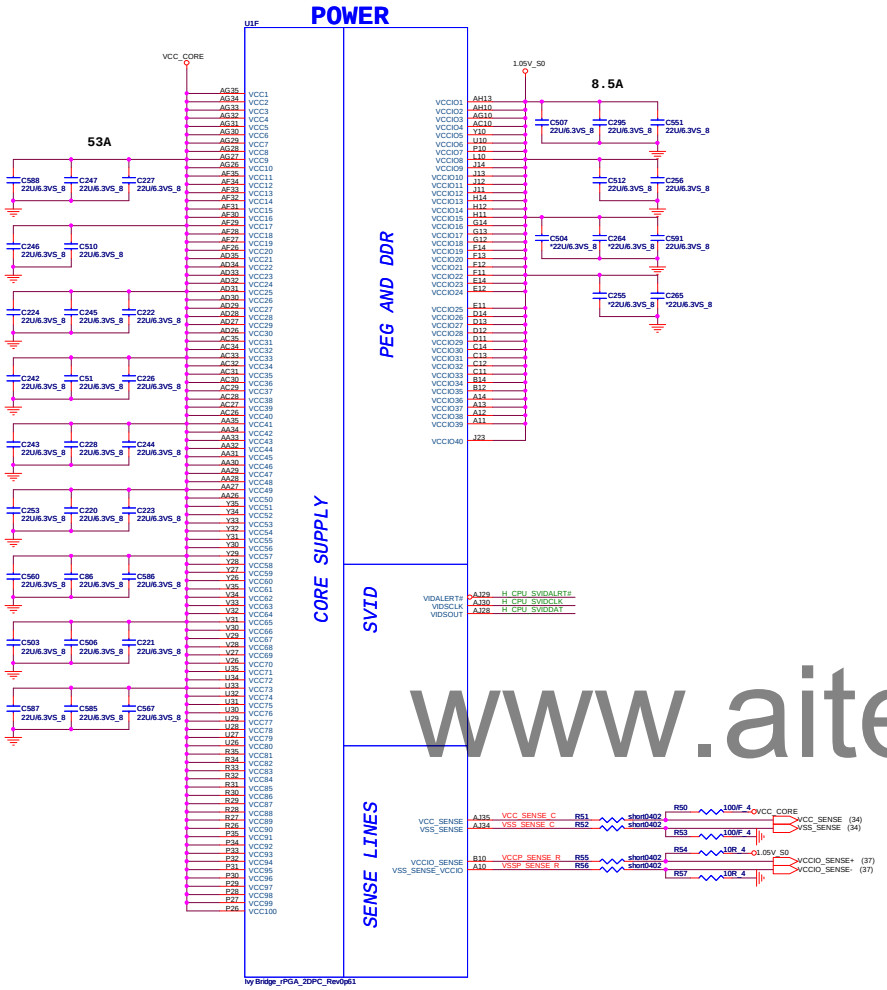
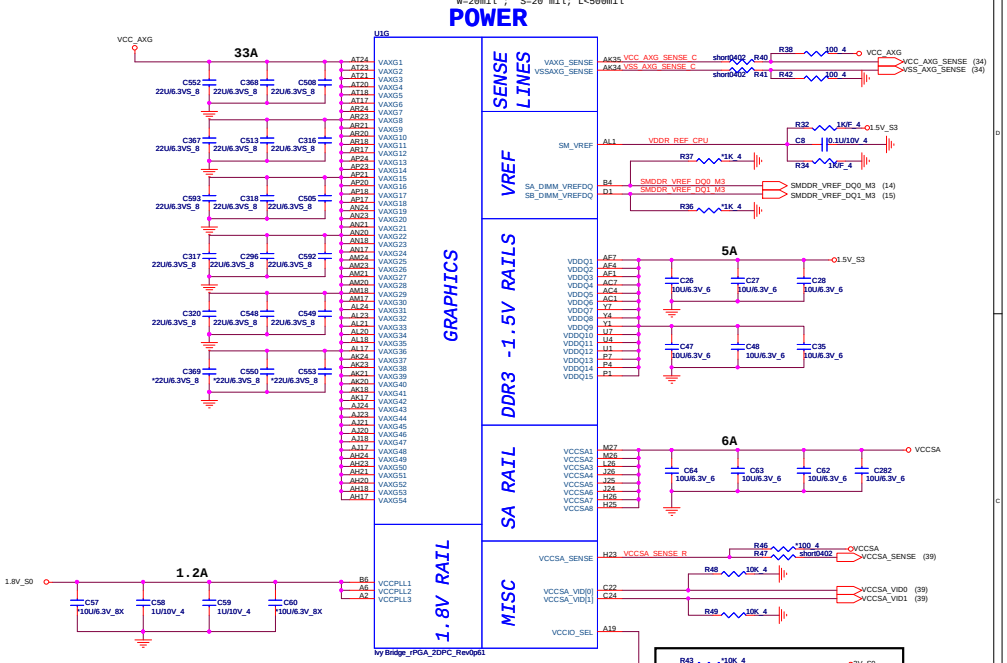
Ivy Bridge Processor (POWER)



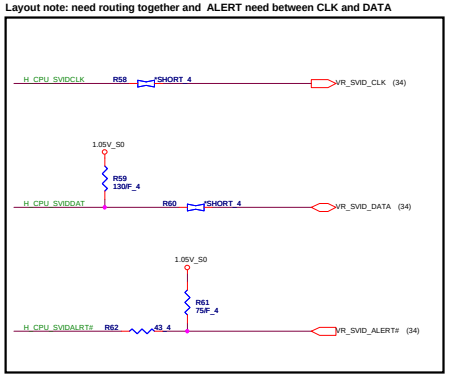
Ivy Bridge Processor (GRAPHIC POWER)

W=20mil ; S=20 mil; L<500mil



VCCIO_SEL	
1	1.05V
0	0V

Layout note: need routing together and ALERT need between CLK and DATA



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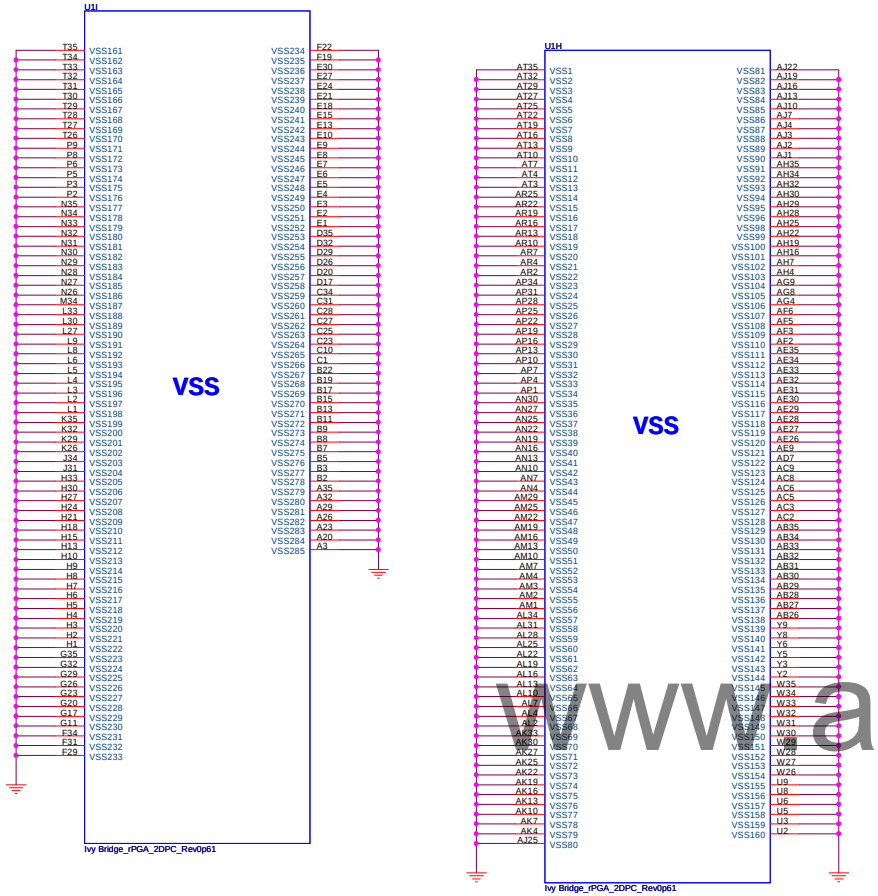
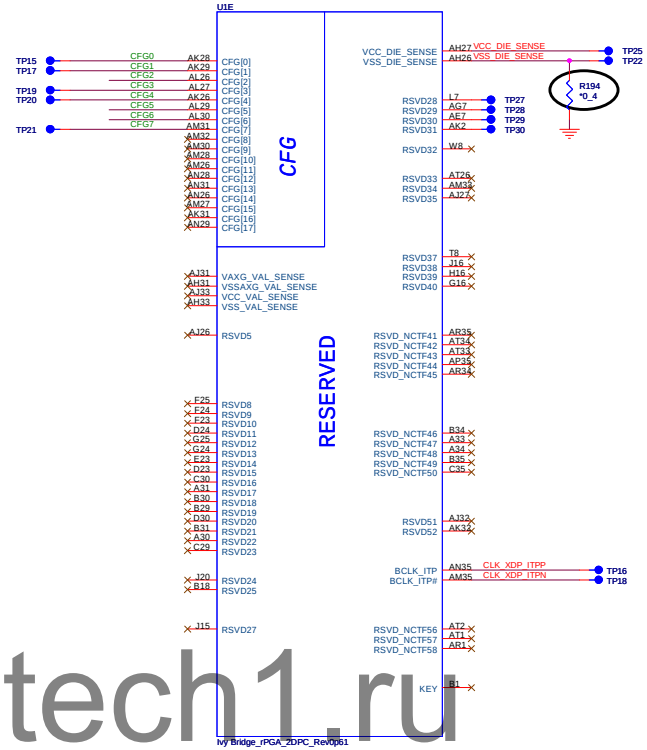
Ivy Bridge Processor (GND)

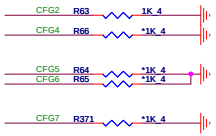


Ivy Bridge Processor (RESERVED, CFG)



Processor Strapping

CFG2	0	PCIe X16 LANE Reversed
	1	Normal Operation
CFG3	0	PCIe X4 LANE Reversed
	1	Normal Operation
CFG4	0	Enable; An ext DP device is connected to eDP
	1	Disable; No physical DP attached to eDP
CFG(5:6)	00	1 x 8 , 2 x 4 PCIe
	01	Reserve
	10	2 x 8 PCIe
	11	1 x 16 PCIe
CFG7	0	PEG Wait for BIOS for training
	1	PEG Train immediately following PLT_RST#



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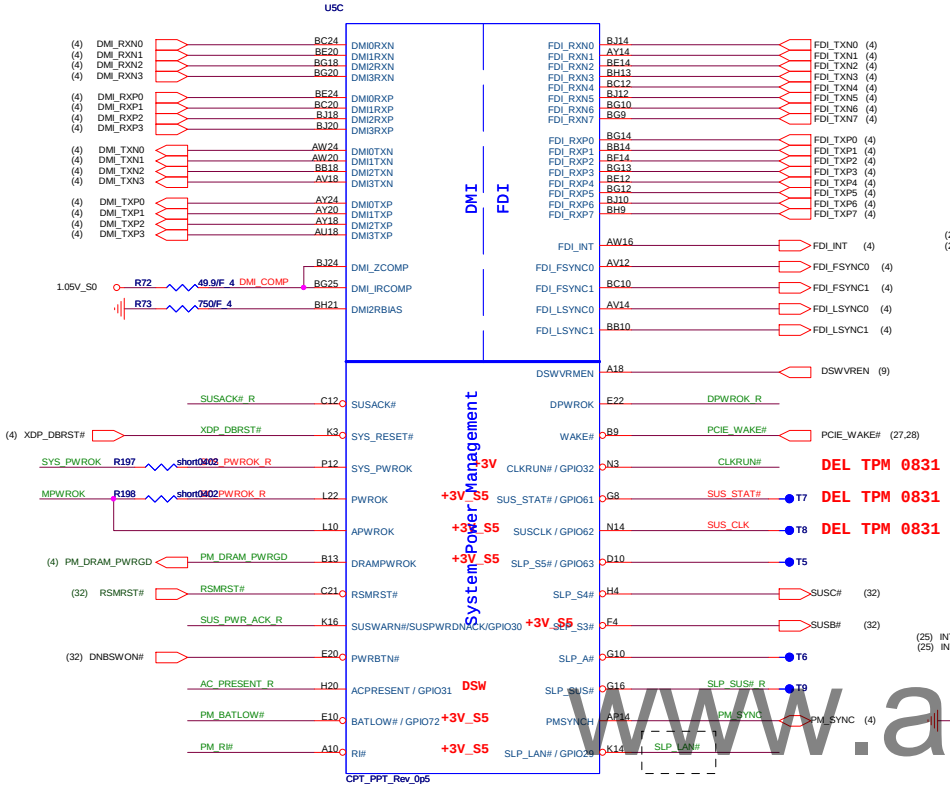
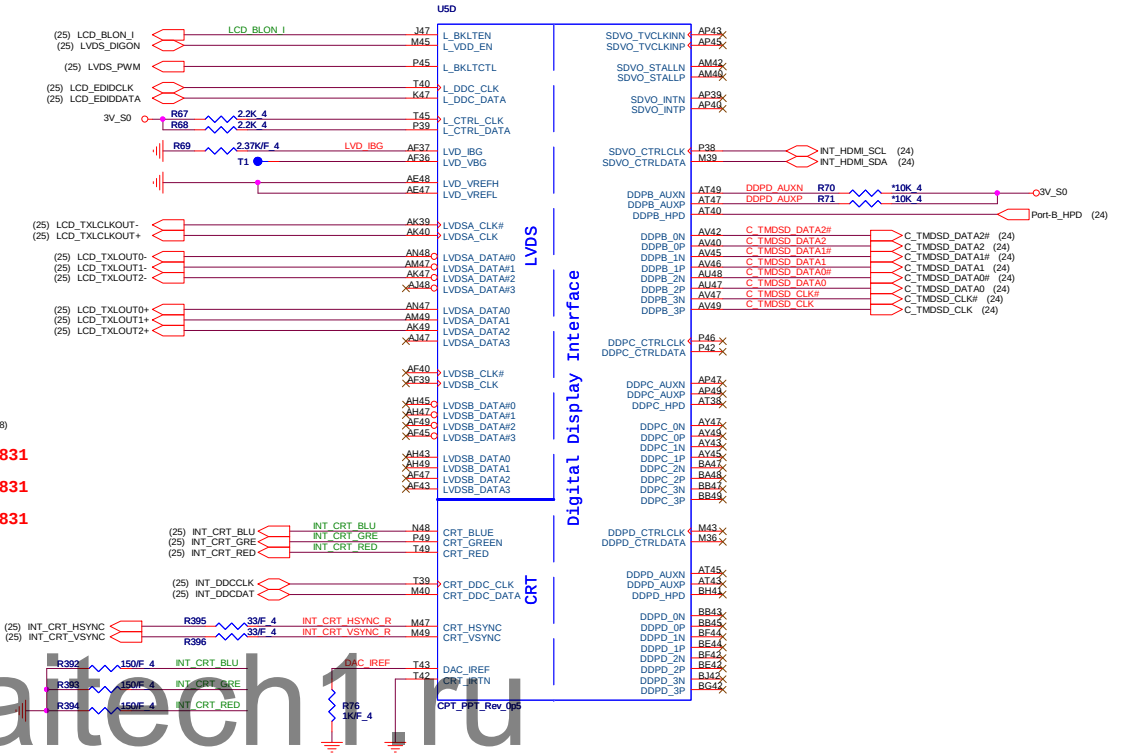
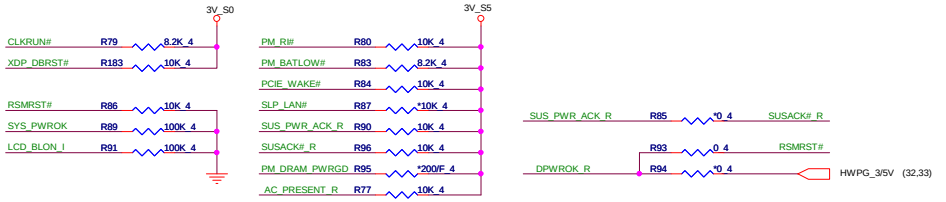
Panther Point (DMI,FDI,PM)



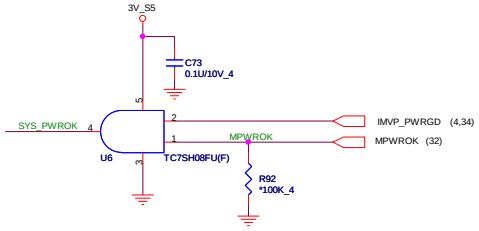
Panther Point (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



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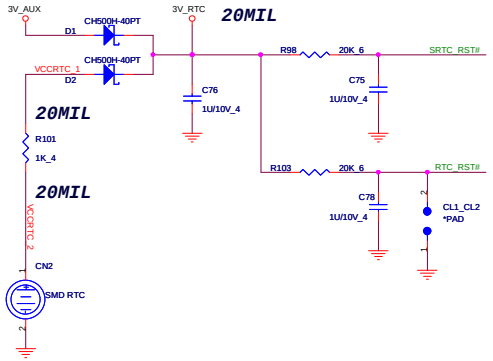
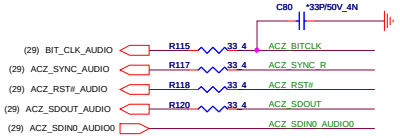
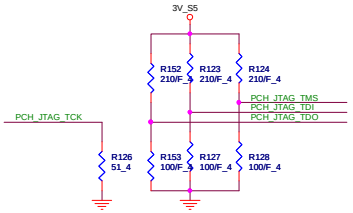
RTC Circuit



HDA Bus



PCH JTAG Debug

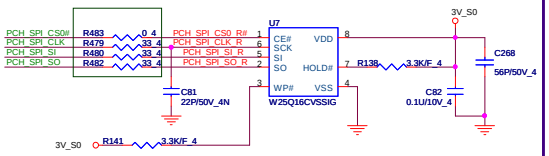


B-12

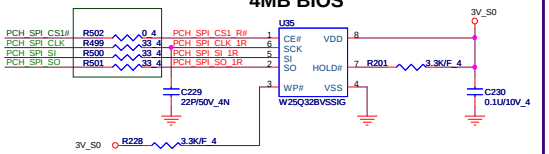
PCH Dual SPI

MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00

2MB ME



4MB BIOS

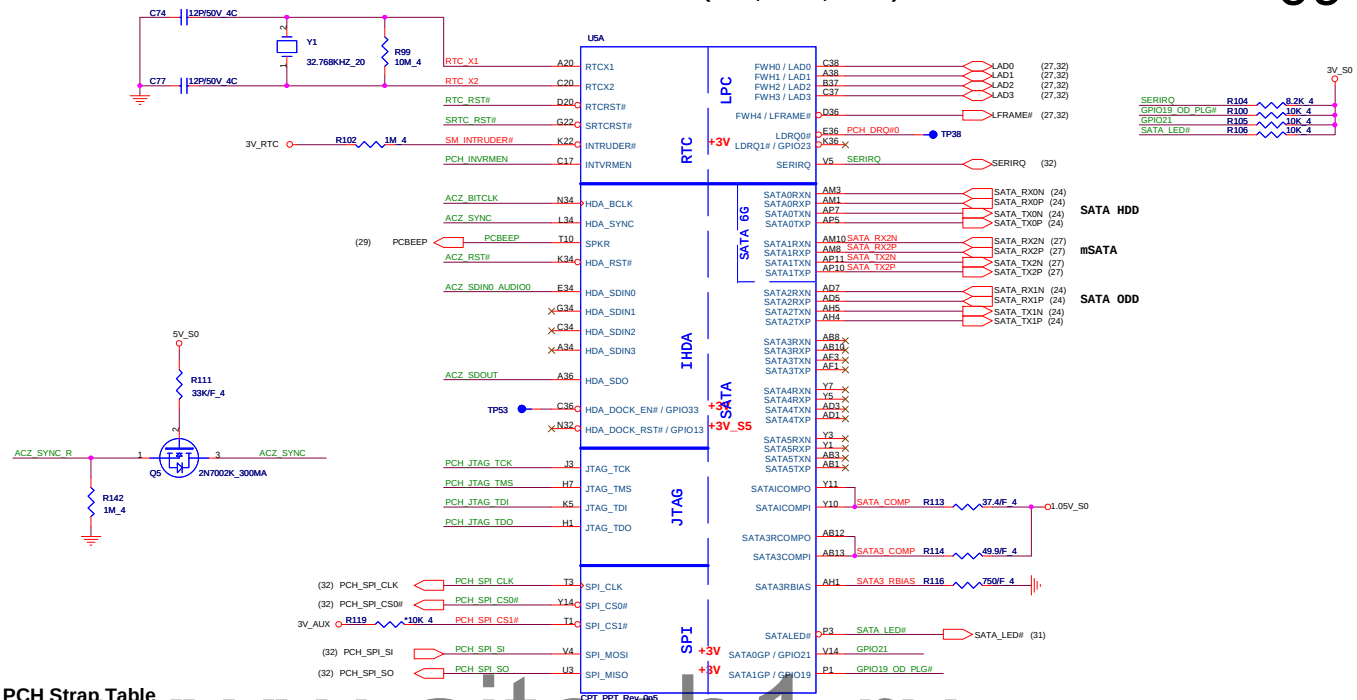


PCH2

1ST BG332768077
2ND BG332768453

Panther Point (HDA,JTAG,SATA)

09



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	3V_S0 R121 *1K_4 PCBEEP
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R122 *1K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	3V_RTC R125 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 / Boot Location 1 / 1 / SPI 0 / 0 / LPC	R129 *1K_4 GNT1# (10) R130 *1K_4 GPIO19_OD_PLG#
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	1 = Override 0 = Default (weak PD 20K)	3V_S0 R131 *1K_4 ACZ_SDOUT ACZ_SDOUT (32)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R132 2.2K_4 R133 1K_4 1.8V_S0 DF_TVS (11) H_SNB_IVB# (4)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	3V_AUX R134 *10K_4 R135 *1K_4 PLL_ODVR_EN (11)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 R136 1K_4 ACZ_SYNC
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	3V_S5 R137 *1K_4 GPIO15 (11)
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	DSWVREN (8) 3V_RTC R139 330K_4 R140 *330K_4
INIT3_3V#	**Reserved**	PWROK	1 = Default (weak pull-up 20K)	**Should not pull low. leave as No Connect**
GNT2#/ GPIO53	**ESI Strap (Server Only)**	PWROK	1 = Default. Should not be pulled low for desktop and mobile	**Should not pull low for desktop and mobile**
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GP/ GPIO37	**Reserved**	PWROK	0 = Default	**Should not be pulled high when strap is sampled**
SATA2GP/ GPIO36	**Reserved**	PWROK	0 = Default	**Should not be pulled high when strap is sampled**

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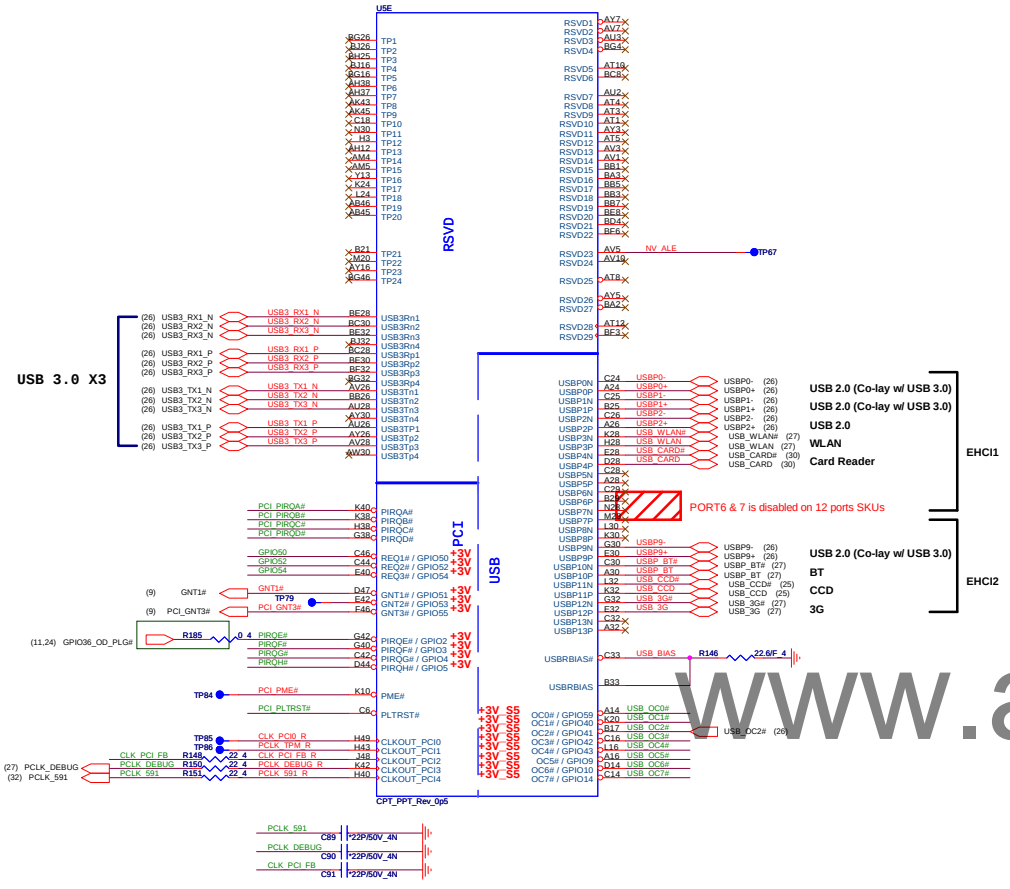
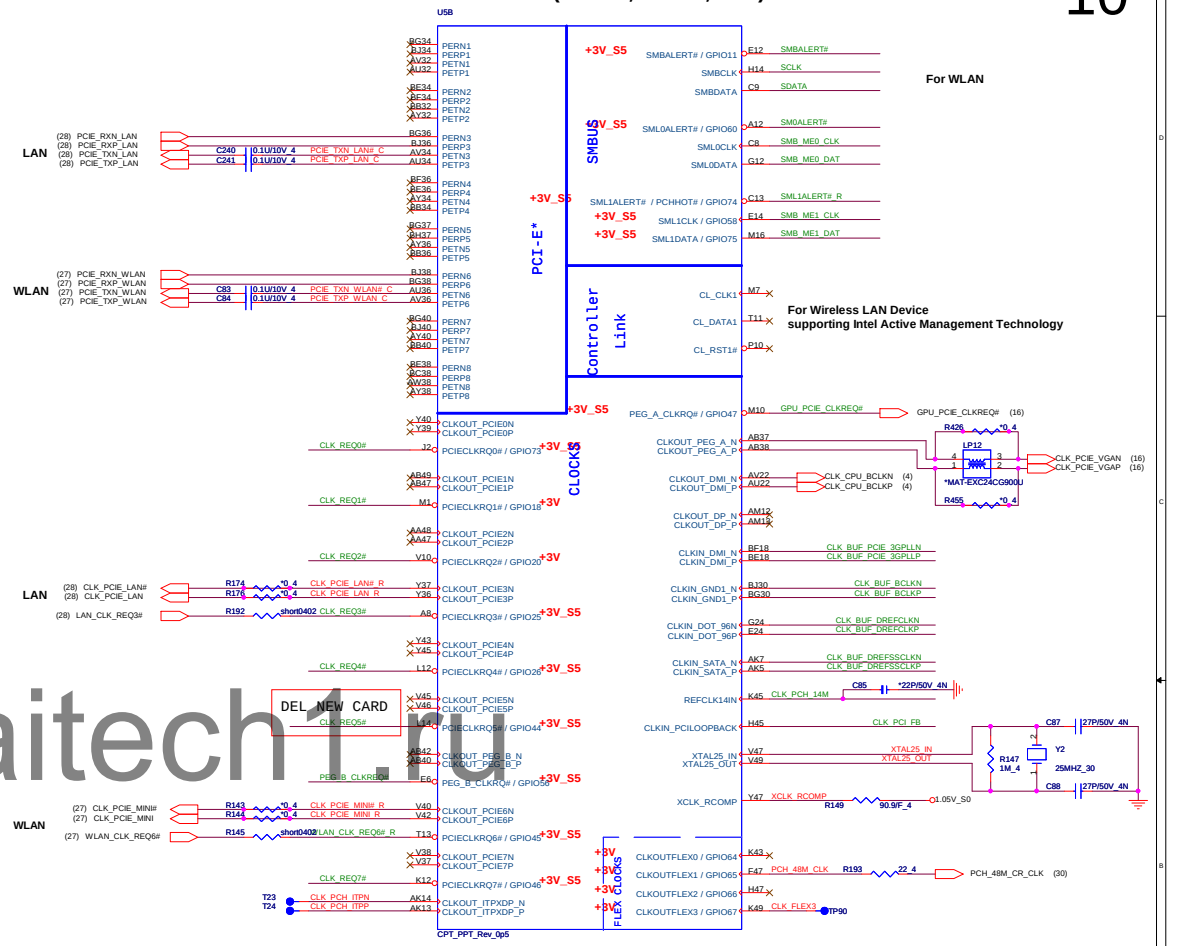
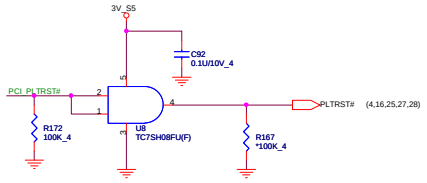
Panther Point-M (PCI,USB,NVRAM)



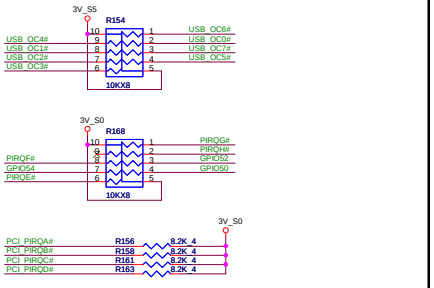
Panther Point-M (PCI-E,SMBUS,CLK)



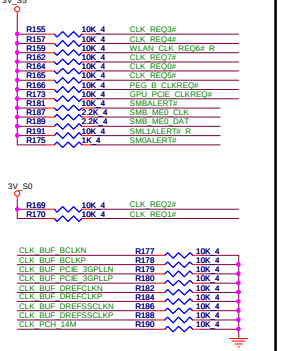
PLTRST#



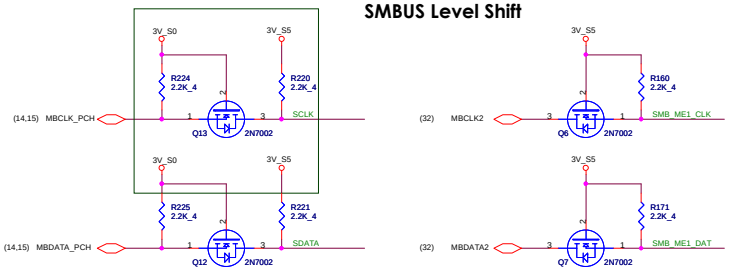
PCI/USBOC# PU



System PU



SMBUS Level Shift



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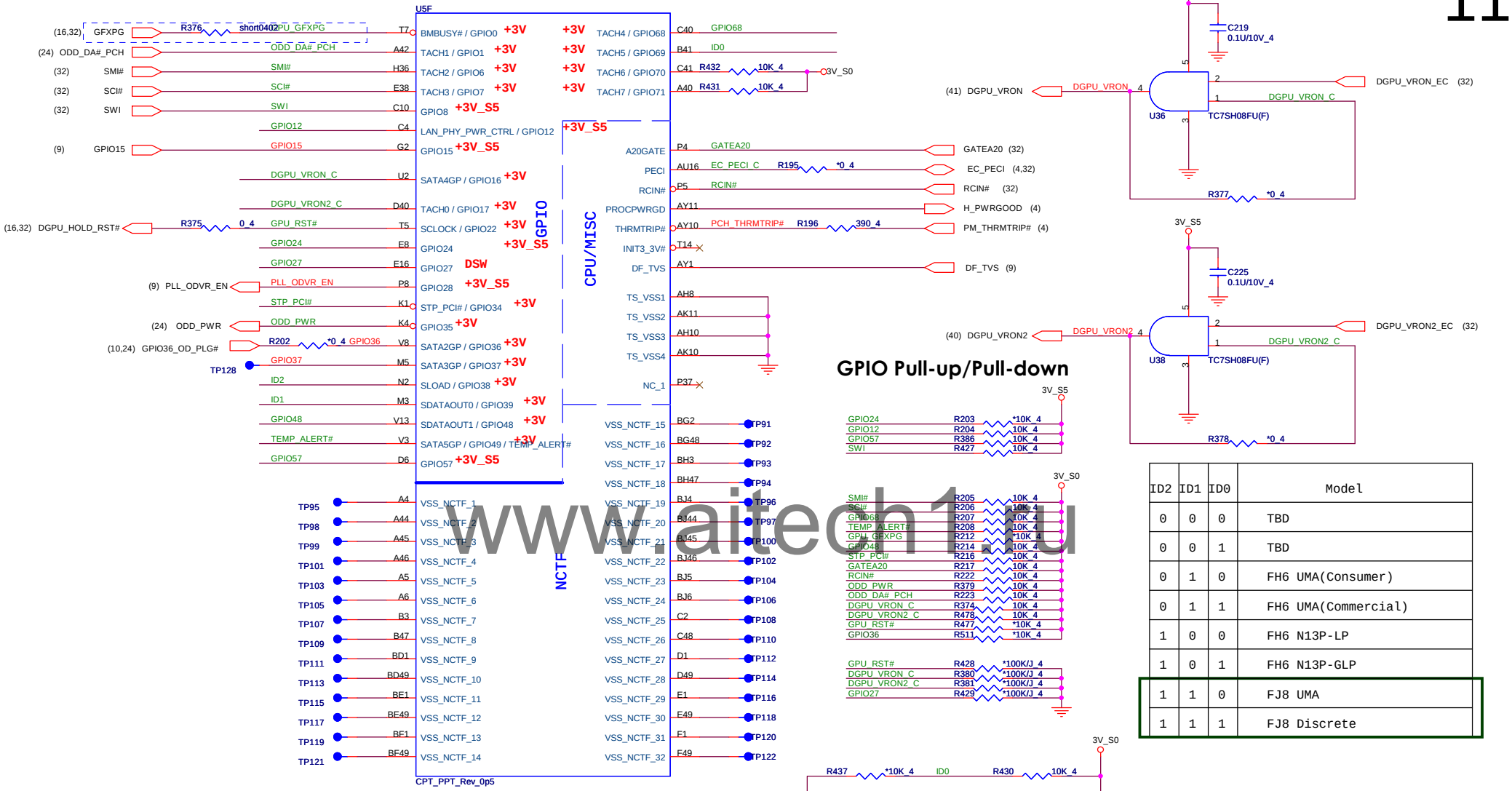
Panther Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down

ID2	ID1	ID0	Model
0	0	0	TBD
0	0	1	TBD
0	1	0	FH6 UMA(Consumer)
0	1	1	FH6 UMA(Commercial)
1	0	0	FH6 N13P-LP
1	0	1	FH6 N13P-GLP
1	1	0	FJ8 UMA
1	1	1	FJ8 Discrete

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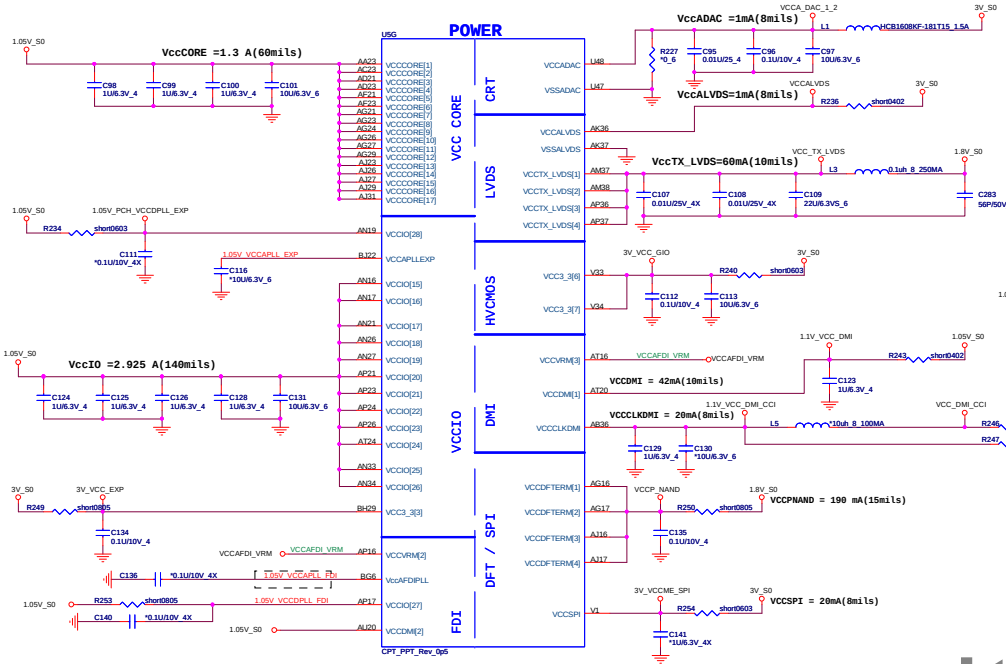
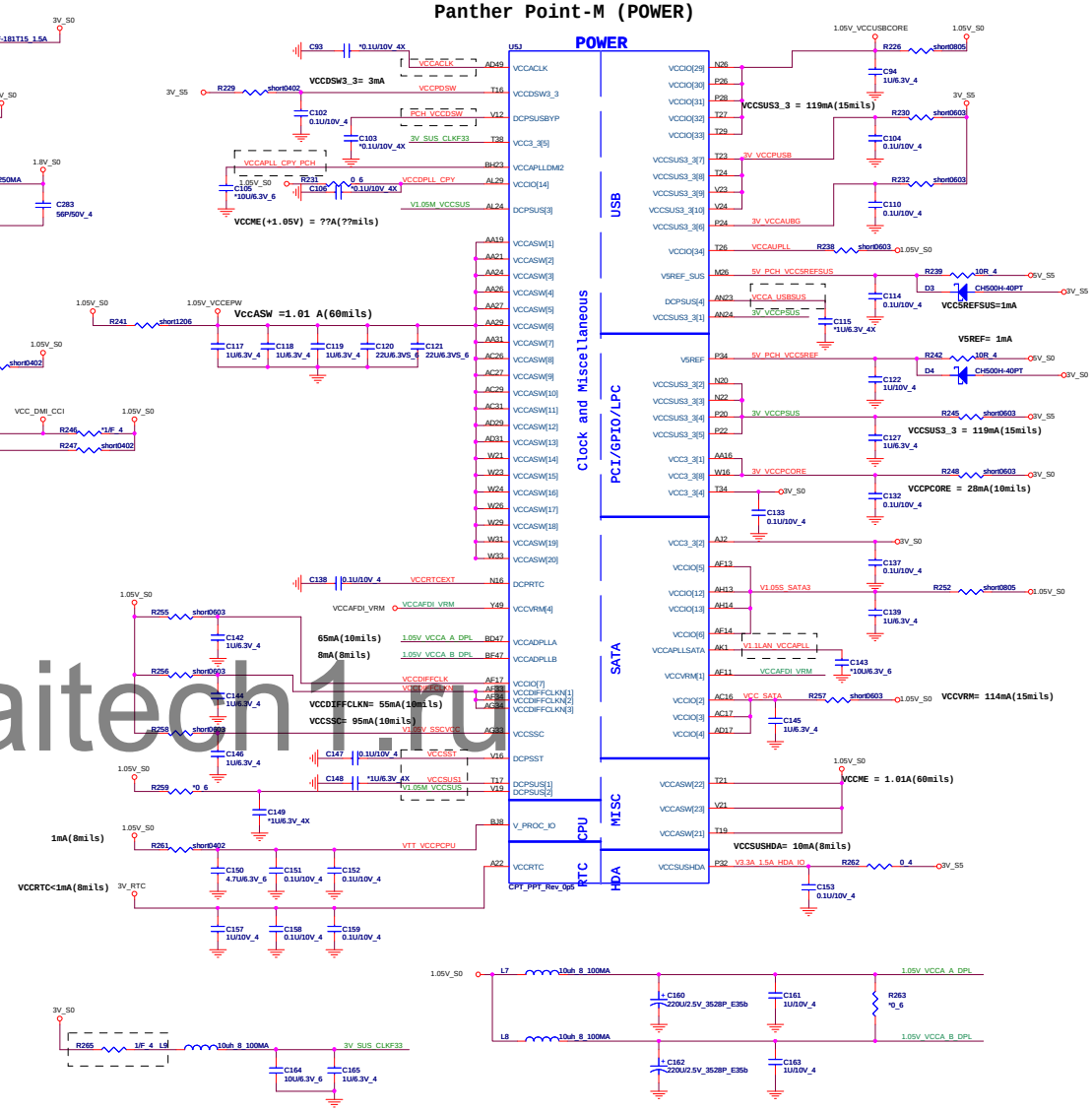
Panther Point (POWER)



Panther Point-M (POWER)



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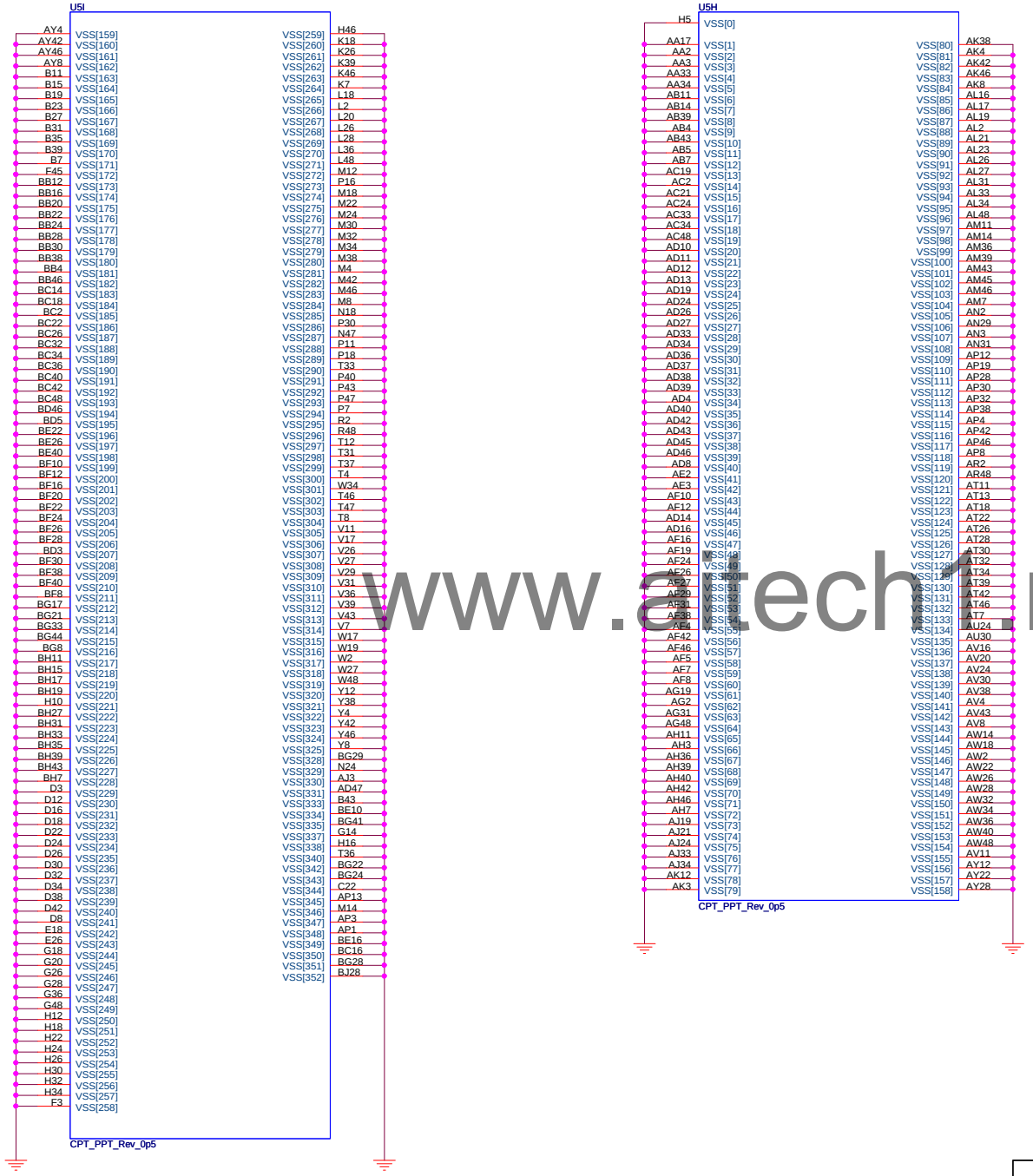
IBEX PEAK-M (GND)



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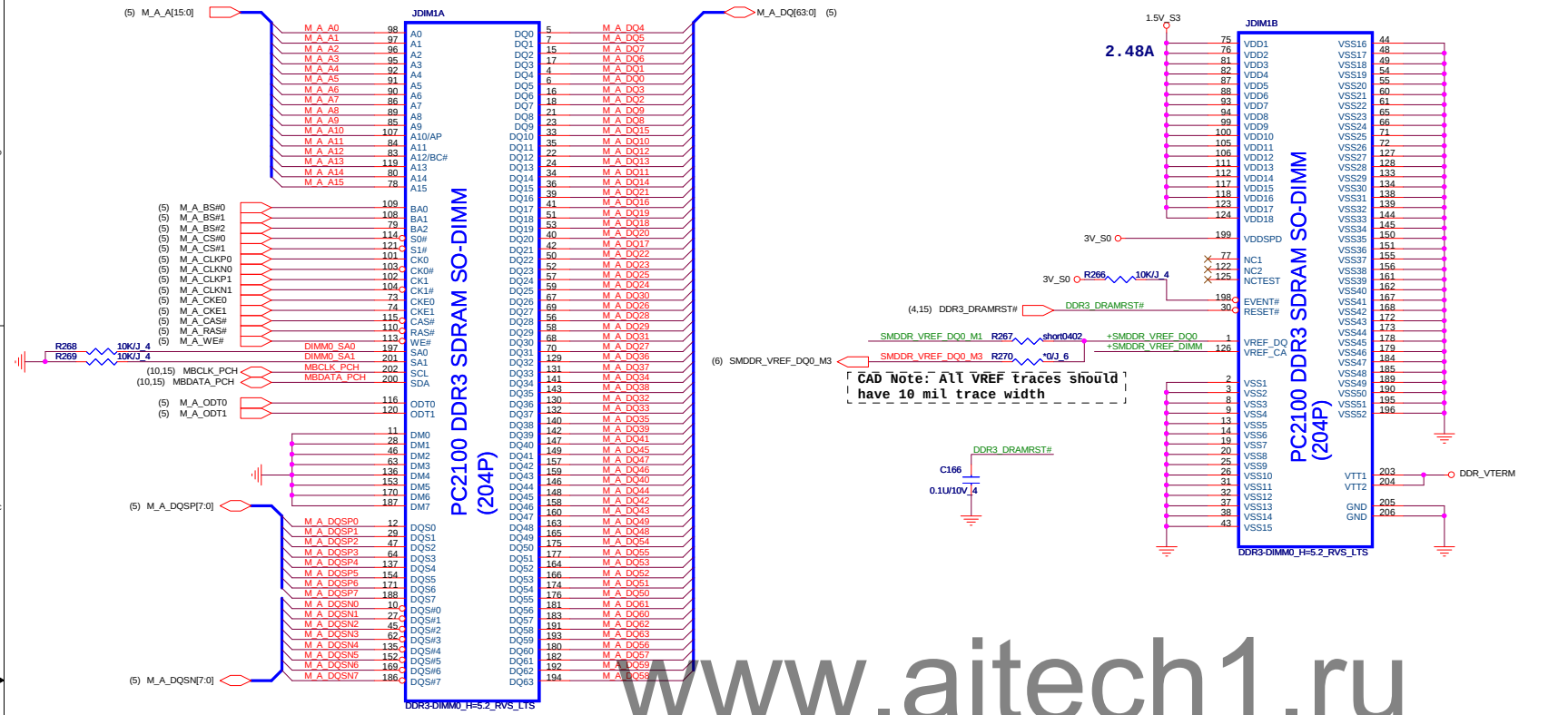
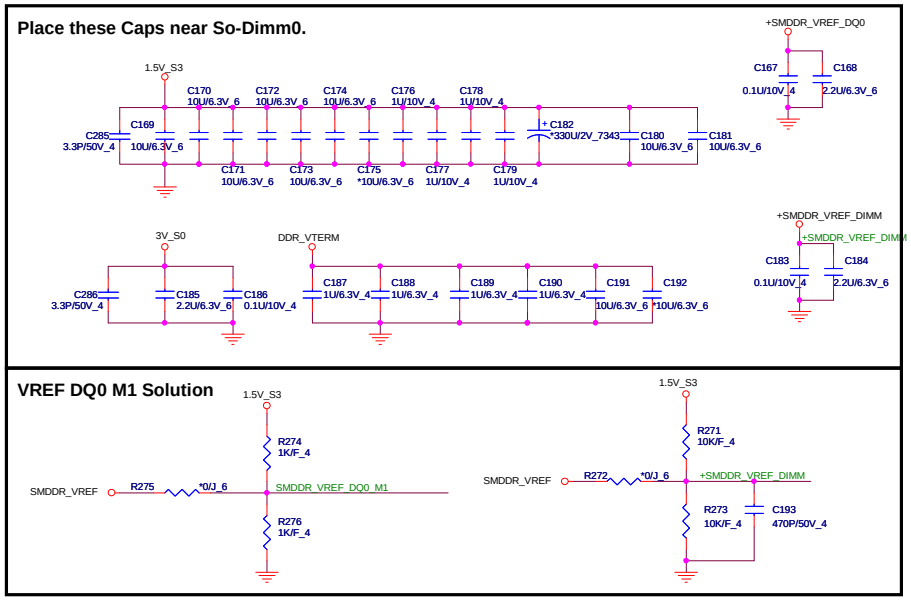
DDR3_RVS





Quanta Computer Inc.		
PROJECT : FJ8		
Size	Document Number: DDRIII SO-DIMM-0	Rev: 2A
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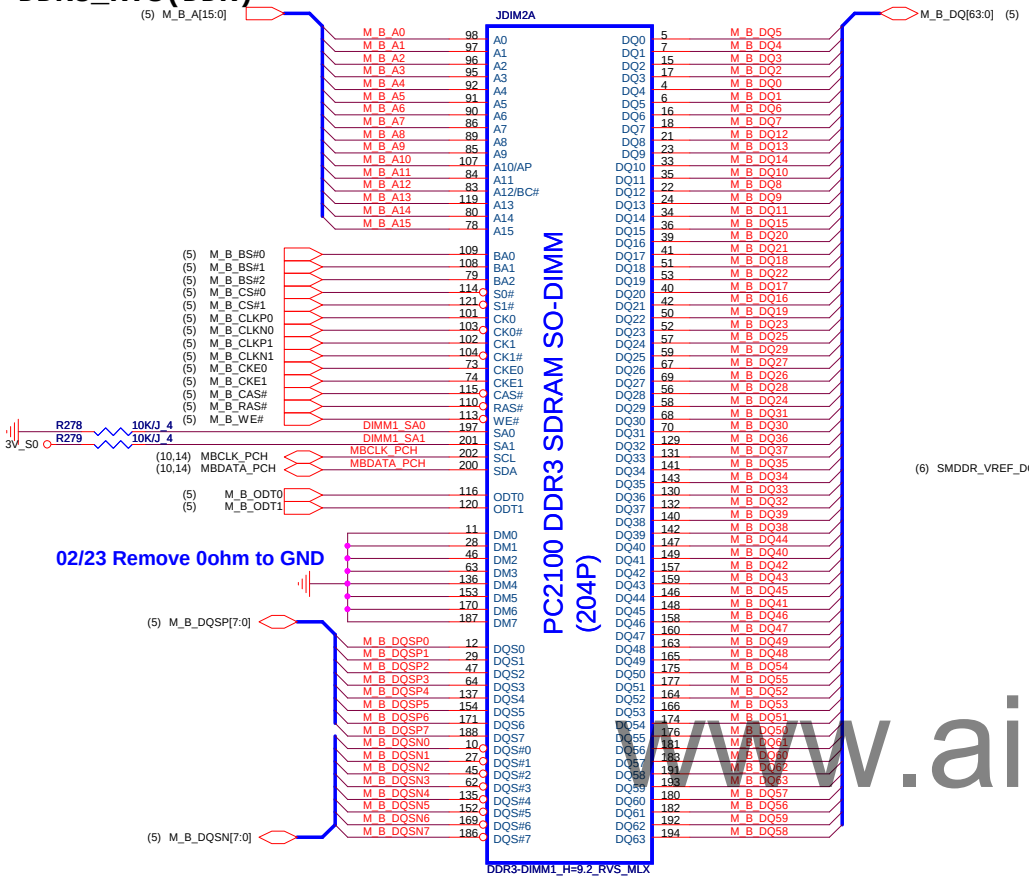
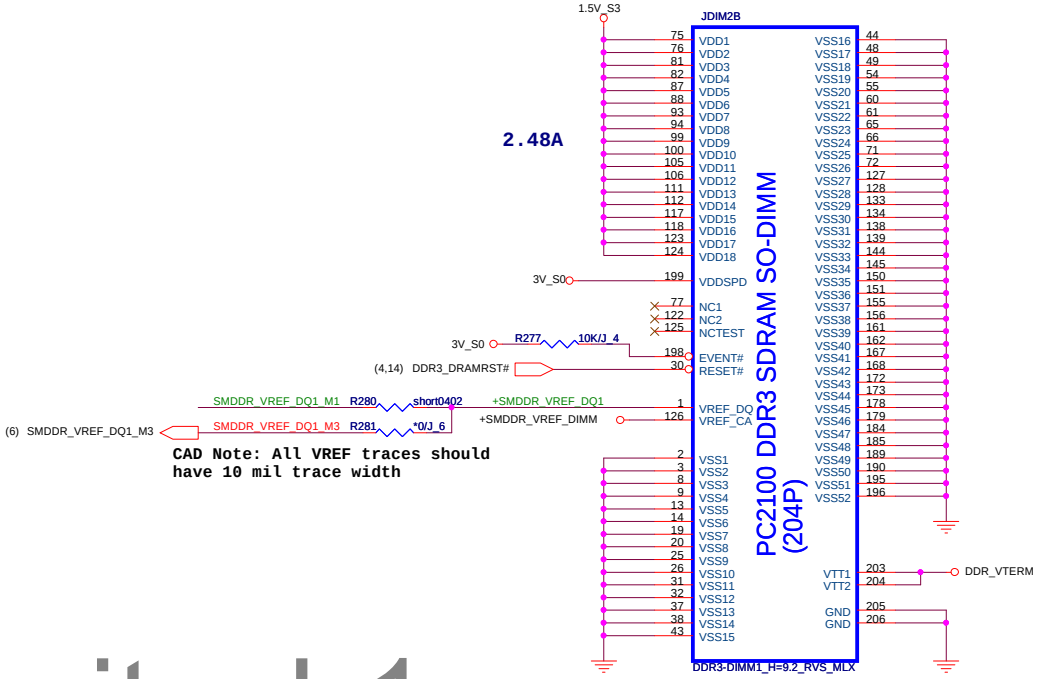
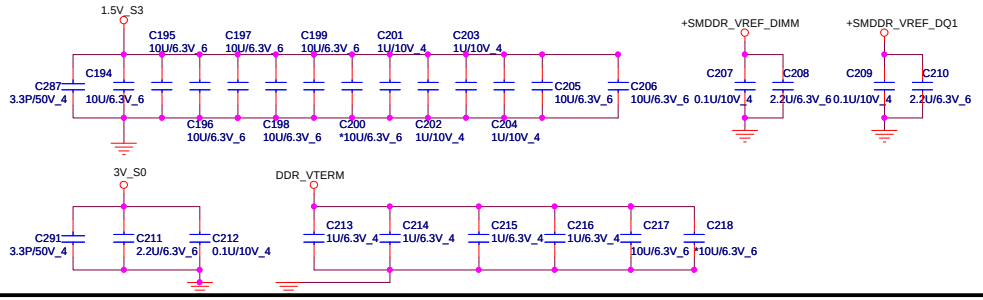
DDR3_RVS(DDR)

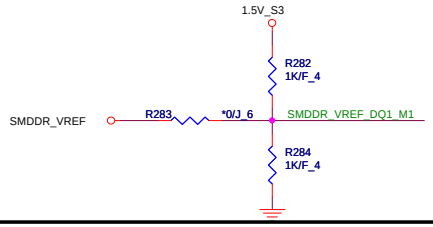




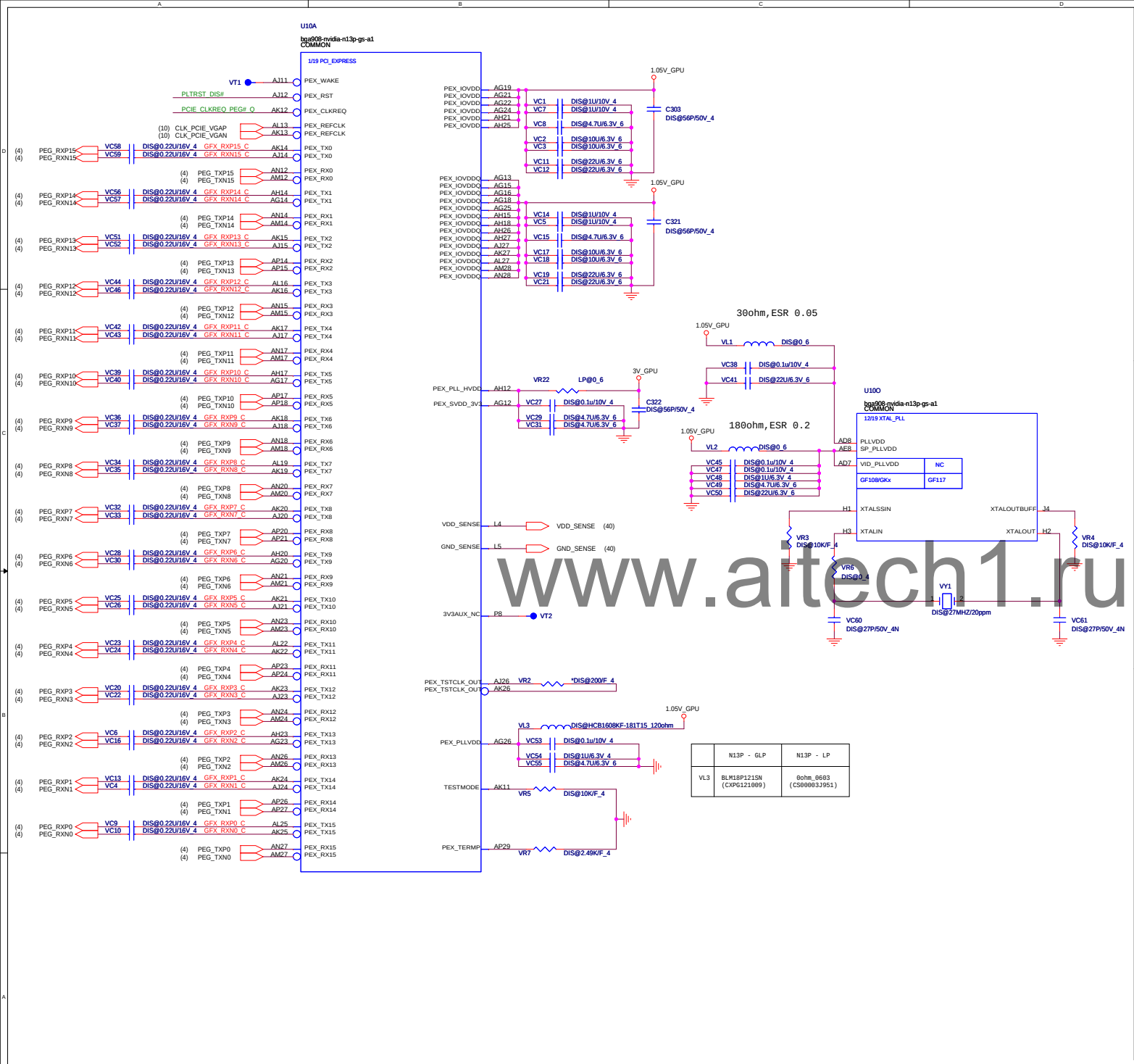
Place these Caps near So-Dimm1.



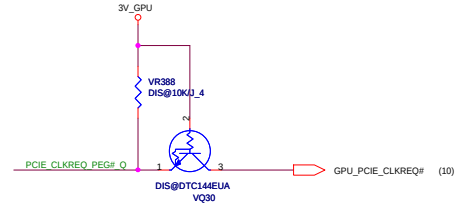
VREF DQ1 M1 Solution



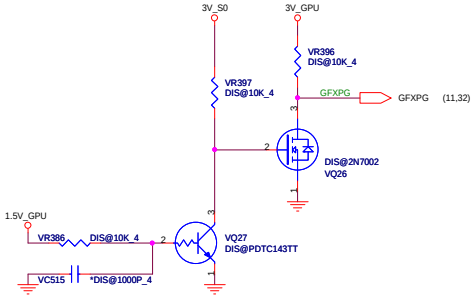
Quanta Computer Inc.		
PROJECT : FJ8		
Size	Document Number: DDRIII SO-DIMM-1	Rev: 1A
Date: Monday, January 02, 2012	Sheet 15 of 44	



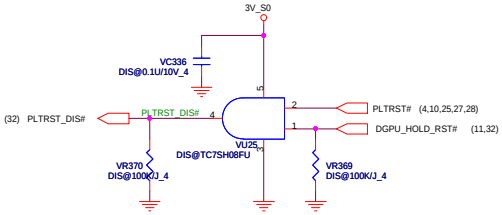
CLK REQ



GPU all PWROK



GPU RST#



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	N13P PCIE	2A

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(22) FBA_DQ[0..63]
(22) FBA_DQM[0..7]
(22) FBA_WDQSP[0..7]
(22) FBA_RDQSN[0..7]
(22) FBA_CMD[0..31]

(23) FBB_DQ[0..63]
(23) FBB_DQM[0..7]
(23) FBB_WDQSP[0..7]
(23) FBB_RDQSN[0..7]
(23) FBB_CMD[0..31]

U10B
bga908-nvidia-n13p-gs-a1
COMMON
2/19 FBA

U10C
bga908-nvidia-n13p-gs-a1
COMMON
3/19 FBB

	N13P-GLP	N13P-LP
VR111	NA	10Kohm_0402 (CS31002FB26)

VR111 LP@10K/F_4
FB_CLAMP E1
FB_DLL_AVDD K27 FBA_PLL_AVDD
VC62 DIS@0.1u/10V_4

FBA_DQ0 L28 FBA_D0
FBA_DQ1 M29 FBA_D1
FBA_DQ2 L29 FBA_D2
FBA_DQ3 M28 FBA_D3
FBA_DQ4 N31 FBA_D4
FBA_DQ5 P29 FBA_D5
FBA_DQ6 R29 FBA_D6
FBA_DQ7 P28 FBA_D7
FBA_DQ8 J28 FBA_D8
FBA_DQ9 H29 FBA_D9
FBA_DQ10 J29 FBA_D10
FBA_DQ11 H28 FBA_D11
FBA_DQ12 G29 FBA_D12
FBA_DQ13 E31 FBA_D13
FBA_DQ14 E32 FBA_D14
FBA_DQ15 F30 FBA_D15
FBA_DQ16 C34 FBA_D16
FBA_DQ17 D32 FBA_D17
FBA_DQ18 B33 FBA_D18
FBA_DQ19 C33 FBA_D19
FBA_DQ20 F33 FBA_D20
FBA_DQ21 F32 FBA_D21
FBA_DQ22 H33 FBA_D22
FBA_DQ23 H32 FBA_D23
FBA_DQ24 P34 FBA_D24
FBA_DQ25 P32 FBA_D25
FBA_DQ26 P31 FBA_D26
FBA_DQ27 P33 FBA_D27
FBA_DQ28 L31 FBA_D28
FBA_DQ29 L34 FBA_D29
FBA_DQ30 L32 FBA_D30
FBA_DQ31 L33 FBA_D31
FBA_DQ32 AG28 FBA_D32
FBA_DQ33 AF29 FBA_D33
FBA_DQ34 AG29 FBA_D34
FBA_DQ35 AF28 FBA_D35
FBA_DQ36 AD30 FBA_D36
FBA_DQ37 AD29 FBA_D37
FBA_DQ38 AC29 FBA_D38
FBA_DQ39 AD28 FBA_D39
FBA_DQ40 AJ29 FBA_D40
FBA_DQ41 AK29 FBA_D41
FBA_DQ42 AJ30 FBA_D42
FBA_DQ43 AK28 FBA_D43
FBA_DQ44 AM29 FBA_D44
FBA_DQ45 AM31 FBA_D45
FBA_DQ46 AN29 FBA_D46
FBA_DQ47 AM30 FBA_D47
FBA_DQ48 AN31 FBA_D48
FBA_DQ49 AN32 FBA_D49
FBA_DQ50 AP30 FBA_D50
FBA_DQ51 AP32 FBA_D51
FBA_DQ52 AM33 FBA_D52
FBA_DQ53 AL31 FBA_D53
FBA_DQ54 AK33 FBA_D54
FBA_DQ55 AK32 FBA_D55
FBA_DQ56 AD34 FBA_D56
FBA_DQ57 AD32 FBA_D57
FBA_DQ58 AC30 FBA_D58
FBA_DQ59 AD33 FBA_D59
FBA_DQ60 AF31 FBA_D60
FBA_DQ61 AG34 FBA_D61
FBA_DQ62 AG32 FBA_D62
FBA_DQ63 AG33 FBA_D63

FBA_DQM0 P30 FBA_DQM0
FBA_DQM1 F31 FBA_DQM1
FBA_DQM2 F34 FBA_DQM2
FBA_DQM3 M32 FBA_DQM3
FBA_DQM4 AD31 FBA_DQM4
FBA_DQM5 AL29 FBA_DQM5
FBA_DQM6 AM32 FBA_DQM6
FBA_DQM7 AF34 FBA_DQM7

FBA_WDQSP0 M31 FBA_DQS_WP0
FBA_WDQSP1 G31 FBA_DQS_WP1
FBA_WDQSP2 E33 FBA_DQS_WP2
FBA_WDQSP3 M33 FBA_DQS_WP3
FBA_WDQSP4 AE31 FBA_DQS_WP4
FBA_WDQSP5 AK30 FBA_DQS_WP5
FBA_WDQSP6 AN33 FBA_DQS_WP6
FBA_WDQSP7 AF33 FBA_DQS_WP7

FBA_RDQSN0 M30 FBA_DQS_RN0
FBA_RDQSN1 H30 FBA_DQS_RN1
FBA_RDQSN2 E34 FBA_DQS_RN2
FBA_RDQSN3 M34 FBA_DQS_RN3
FBA_RDQSN4 AF30 FBA_DQS_RN4
FBA_RDQSN5 AK31 FBA_DQS_RN5
FBA_RDQSN6 AM34 FBA_DQS_RN6
FBA_RDQSN7 AF32 FBA_DQS_RN7

H26 FB_VREF

FBA_CMD0 U30 FBA_CMD0
FBA_CMD1 T31 FBA_CMD1
FBA_CMD2 U29 FBA_CMD2
FBA_CMD3 R34 FBA_CMD3
FBA_CMD4 R33 FBA_CMD4
FBA_CMD5 U32 FBA_CMD5
FBA_CMD6 U33 FBA_CMD6
FBA_CMD7 U28 FBA_CMD7
FBA_CMD8 V28 FBA_CMD8
FBA_CMD9 V29 FBA_CMD9
FBA_CMD10 V30 FBA_CMD10
FBA_CMD11 U34 FBA_CMD11
FBA_CMD12 U31 FBA_CMD12
FBA_CMD13 V34 FBA_CMD13
FBA_CMD14 V33 FBA_CMD14
FBA_CMD15 V32 FBA_CMD15
FBA_CMD16 AA31 FBA_CMD16
FBA_CMD17 AA29 FBA_CMD17
FBA_CMD18 AA28 FBA_CMD18
FBA_CMD19 AC34 FBA_CMD19
FBA_CMD20 AC33 FBA_CMD20
FBA_CMD21 AA32 FBA_CMD21
FBA_CMD22 AA33 FBA_CMD22
FBA_CMD23 Y28 FBA_CMD23
FBA_CMD24 Y29 FBA_CMD24
FBA_CMD25 W31 FBA_CMD25
FBA_CMD26 Y30 FBA_CMD26
FBA_CMD27 AA34 FBA_CMD27
FBA_CMD28 Y31 FBA_CMD28
FBA_CMD29 Y34 FBA_CMD29
FBA_CMD30 Y33 FBA_CMD30
FBA_CMD31 V31 FBA_CMD31

VT3
VT5
VT7

FBA_CMD_RFU0 R32
FBA_CMD_RFU1 AC32
VT9
VT10

FBA_DEBUG0 R28 FBA_DEBUG0
FBA_DEBUG1 AC28 FBA_DEBUG1
VR18 *DIS@60.4/F_4
VR19 *DIS@60.4/F_4
1.5V_GPU

FBA_CLK0 R30
FBA_CLK0 R31
FBA_CLK1 AB31
FBA_CLK1 AC31
FBA_CLK0 (22)
FBA_CLK#0 (22)
FBA_CLK1 (22)
FBA_CLK#1 (22)

FBA_WCK01 K31
FBA_WCK01 L30
FBA_WCK23 H34
FBA_WCK23 J34
FBA_WCK45 AG30
FBA_WCK45 AG31
FBA_WCK67 AJ34
FBA_WCK67 AK34

FBA_WCKB01 J30
FBA_WCKB01 J31
FBA_WCKB23 J32
FBA_WCKB23 J33
FBA_WCKB45 AH31
FBA_WCKB45 AJ31
FBA_WCKB67 AJ32
FBA_WCKB67 AJ33

FBA_PLL_AVDD U27 FBA_PLL_AVDD
VL4 DIS@bead_30ohm_6
1.05V_GPU
VC64 DIS@0.1u/10V_4
VC65 DIS@22u/6.3V_6

FBA_CMD2 VR8 DIS@10K_4 FBA_ODT_L
FBA_CMD18 VR10 DIS@10K_4 FBA_ODT_H
FBA_CMD3 VR12 DIS@10K_4 FBA_CKE_L
FBA_CMD19 VR14 DIS@10K_4 FBA_CKE_H
FBA_CMD5 VR16 DIS@10K_4 FBA_RST#

FBB_DQ0 G9 FBB_D0
FBB_DQ1 E9 FBB_D1
FBB_DQ2 G8 FBB_D2
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FBB_DQ5 G11 FBB_D5
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FBB_DQ47 D30 FBB_D47
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FBB_DQ49 G31 FBB_D49
FBB_DQ50 E32 FBB_D50
FBB_DQ51 B32 FBB_D51
FBB_DQ52 D29 FBB_D52
FBB_DQ53 A29 FBB_D53
FBB_DQ54 B29 FBB_D54
FBB_DQ55 B26 FBB_D55
FBB_DQ56 B21 FBB_D56
FBB_DQ57 C23 FBB_D57
FBB_DQ58 A21 FBB_D58
FBB_DQ59 C21 FBB_D59
FBB_DQ60 B24 FBB_D60
FBB_DQ61 C24 FBB_D61
FBB_DQ62 B26 FBB_D62
FBB_DQ63 C26 FBB_D63

FBB_DQM0 E11 FBB_DQM0
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FBB_DQM2 A3 FBB_DQM2
FBB_DQM3 C9 FBB_DQM3
FBB_DQM4 F23 FBB_DQM4
FBB_DQM5 F27 FBB_DQM5
FBB_DQM6 C30 FBB_DQM6
FBB_DQM7 A24 FBB_DQM7

FBB_WDQSP0 D10 FBB_DQS_WP0
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FBB_WDQSP5 E28 FBB_DQS_WP5
FBB_WDQSP6 B30 FBB_DQS_WP6
FBB_WDQSP7 A23 FBB_DQS_WP7

FBB_RDQSN0 D9 FBB_DQS_RN0
FBB_RDQSN1 E4 FBB_DQS_RN1
FBB_RDQSN2 B2 FBB_DQS_RN2
FBB_RDQSN3 A9 FBB_DQS_RN3
FBB_RDQSN4 D22 FBB_DQS_RN4
FBB_RDQSN5 D28 FBB_DQS_RN5
FBB_RDQSN6 A30 FBB_DQS_RN6
FBB_RDQSN7 B23 FBB_DQS_RN7

FBB_CMD0 D13 FBB_CMD0
FBB_CMD1 E14 FBB_CMD1
FBB_CMD2 E14 FBB_CMD2
FBB_CMD3 A12 FBB_CMD3
FBB_CMD4 B12 FBB_CMD4
FBB_CMD5 C14 FBB_CMD5
FBB_CMD6 B14 FBB_CMD6
FBB_CMD7 G15 FBB_CMD7
FBB_CMD8 F15 FBB_CMD8
FBB_CMD9 E15 FBB_CMD9
FBB_CMD10 D15 FBB_CMD10
FBB_CMD11 A14 FBB_CMD11
FBB_CMD12 D14 FBB_CMD12
FBB_CMD13 A15 FBB_CMD13
FBB_CMD14 B15 FBB_CMD14
FBB_CMD15 C17 FBB_CMD15
FBB_CMD16 D18 FBB_CMD16
FBB_CMD17 E18 FBB_CMD17
FBB_CMD18 F18 FBB_CMD18
FBB_CMD19 A20 FBB_CMD19
FBB_CMD20 B20 FBB_CMD20
FBB_CMD21 C19 FBB_CMD21
FBB_CMD22 B18 FBB_CMD22
FBB_CMD23 G18 FBB_CMD23
FBB_CMD24 G17 FBB_CMD24
FBB_CMD25 E17 FBB_CMD25
FBB_CMD26 D16 FBB_CMD26
FBB_CMD27 A18 FBB_CMD27
FBB_CMD28 D17 FBB_CMD28
FBB_CMD29 A17 FBB_CMD29
FBB_CMD30 B17 FBB_CMD30
FBB_CMD31 E17 FBB_CMD31

VT4
VT6
VT8

FBB_CMD_RFU0 C12
FBB_CMD_RFU1 C20
VT11
VT12

FBB_DEBUG0 G14 FBB_DEBUG0
FBB_DEBUG1 G20 FBB_DEBUG1
VR20 *DIS@60.4/F_4
VR21 *DIS@60.4/F_4
1.5V_GPU

FBB_CLK0 D12
FBB_CLK0 E12
FBB_CLK1 E20
FBB_CLK1 F20
FBB_CLK0 (23)
FBB_CLK#0 (23)
FBB_CLK1 (23)
FBB_CLK#1 (23)

FBB_WCK01 F8
FBB_WCK01 E8
FBB_WCK23 A5
FBB_WCK23 A6
FBB_WCK45 D24
FBB_WCK45 D25
FBB_WCK67 B27
FBB_WCK67 C27

FBB_WCKB01 D6
FBB_WCKB01 D7
FBB_WCKB23 C6
FBB_WCKB23 B6
FBB_WCKB45 F26
FBB_WCKB45 E26
FBB_WCKB67 A26
FBB_WCKB67 A27

FBB_PLL_AVDD H17 FBA_PLL_AVDD
VC63 LP@0.1u/10V_4

FBB_CMD2 VR9 DIS@10K_4 FBB_ODT_L
FBB_CMD18 VR11 DIS@10K_4 FBB_ODT_H
FBB_CMD3 VR13 DIS@10K_4 FBB_CKE_L
FBB_CMD19 VR15 DIS@10K_4 FBB_CKE_H
FBB_CMD5 VR17 DIS@10K_4 FBB_RST#

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	N13P MEM I/F	2A

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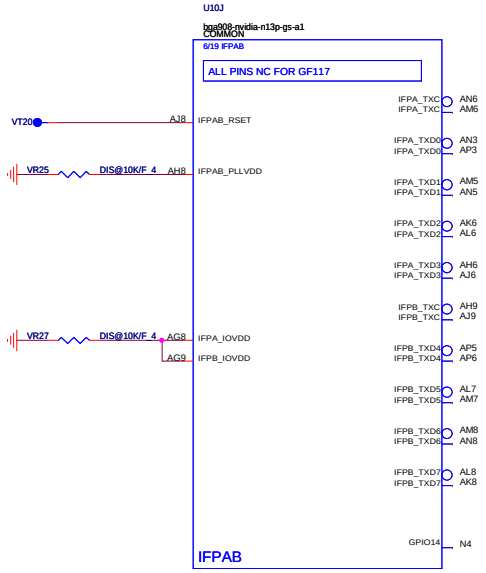
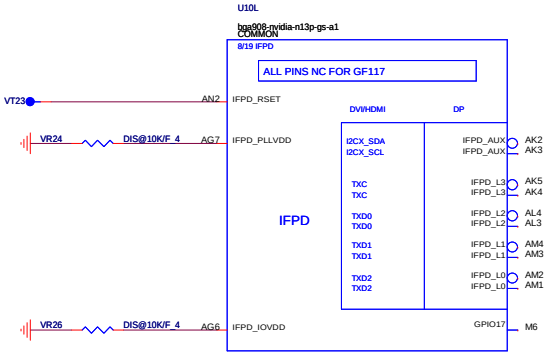
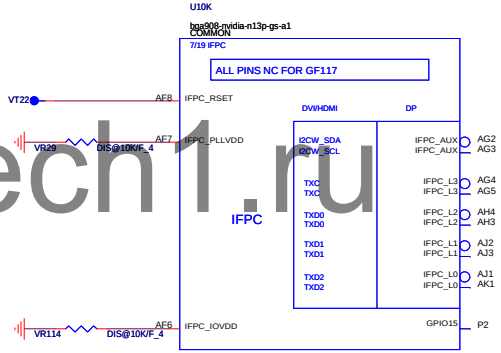
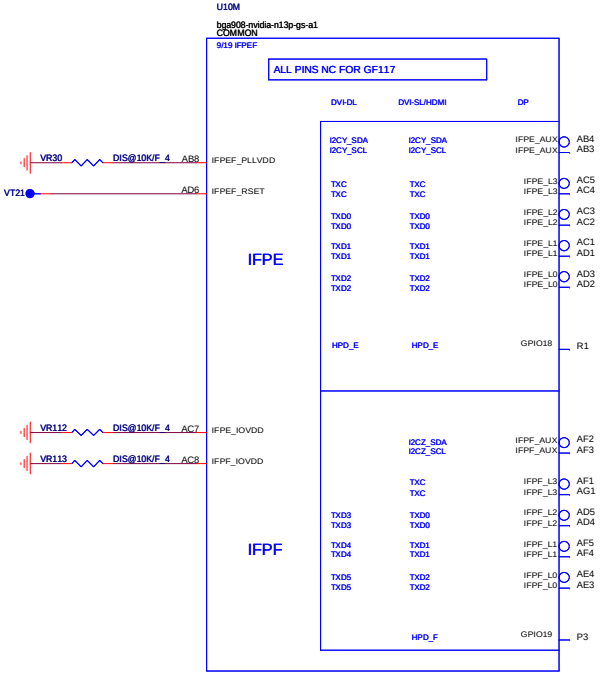
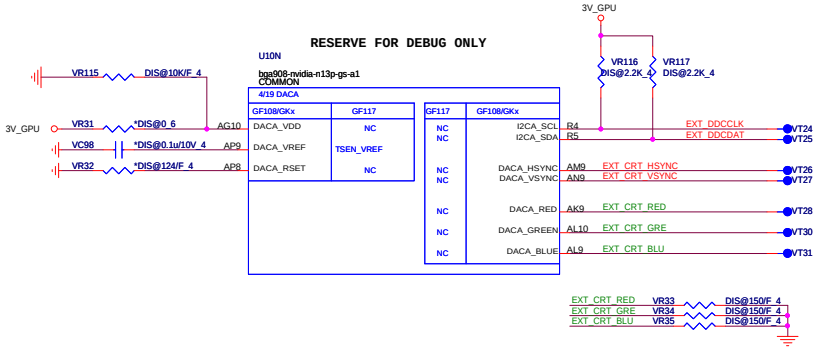








Discrete CRT for Debug



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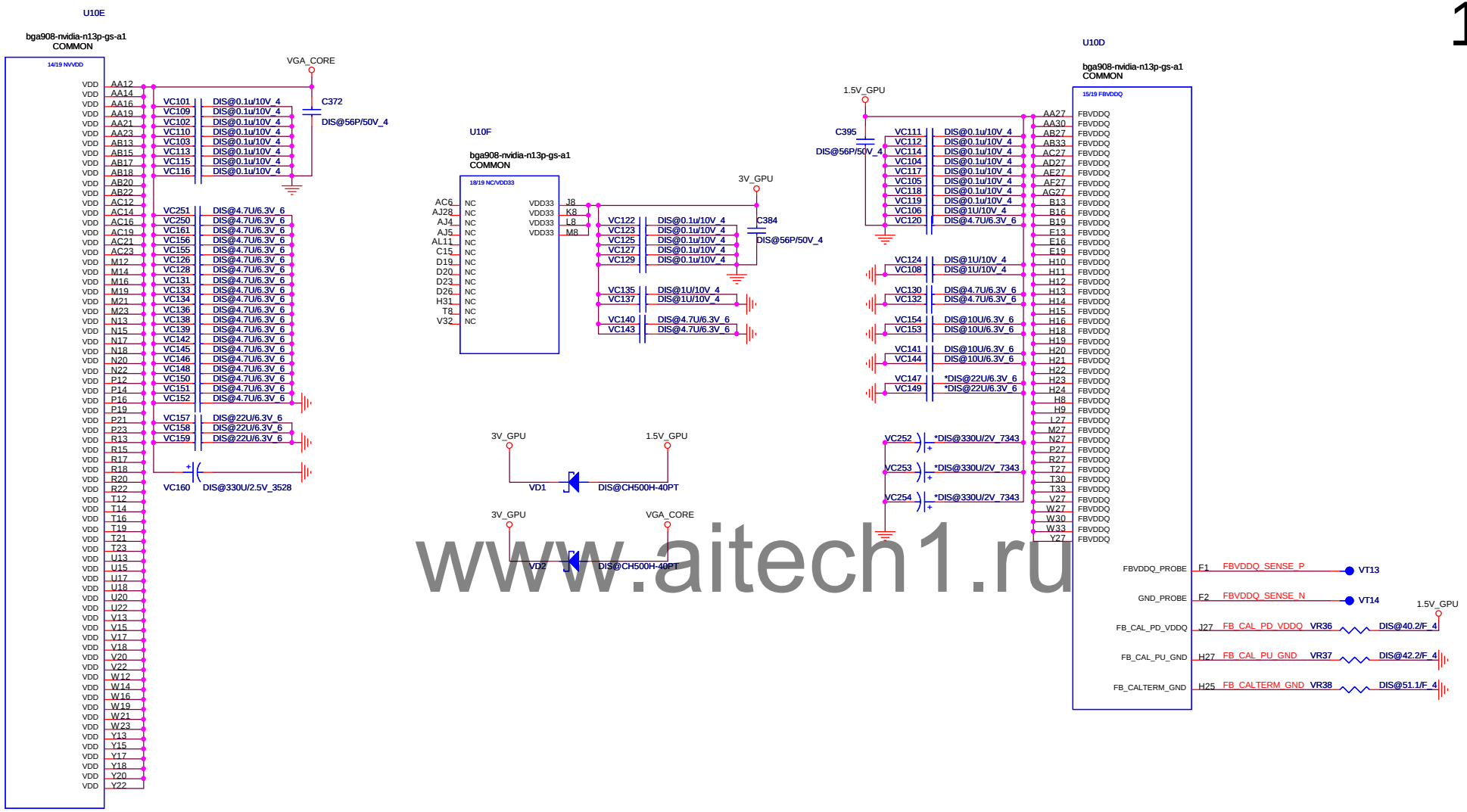
Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	N13P DISPLAY	2A
Date: Monday, January 02, 2012	Sheet 18 of 44	



Quanta Computer Inc.

PROJECT : FJ8

Size	Document Number	Rev
	N13P POWER	2A

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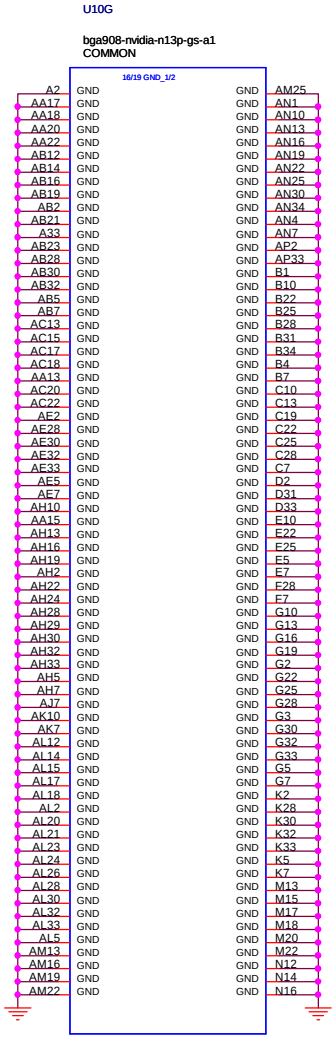

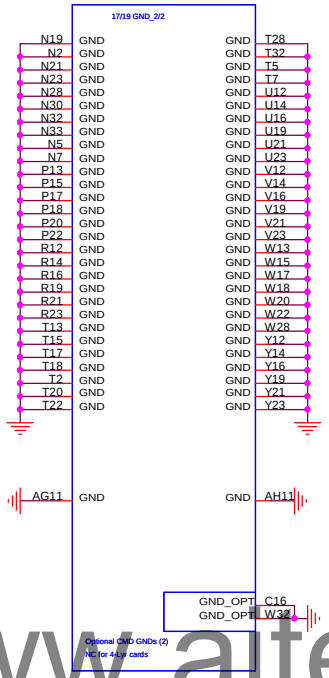

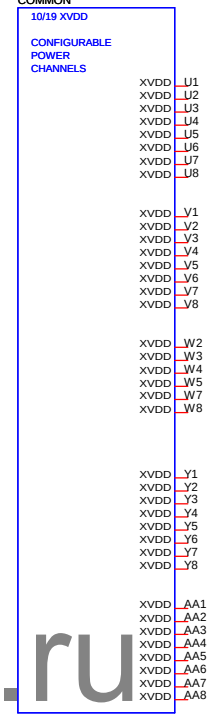

To be configured as needed on the PCB

1.Level 1 Environment-related Substances Should Never be Used.
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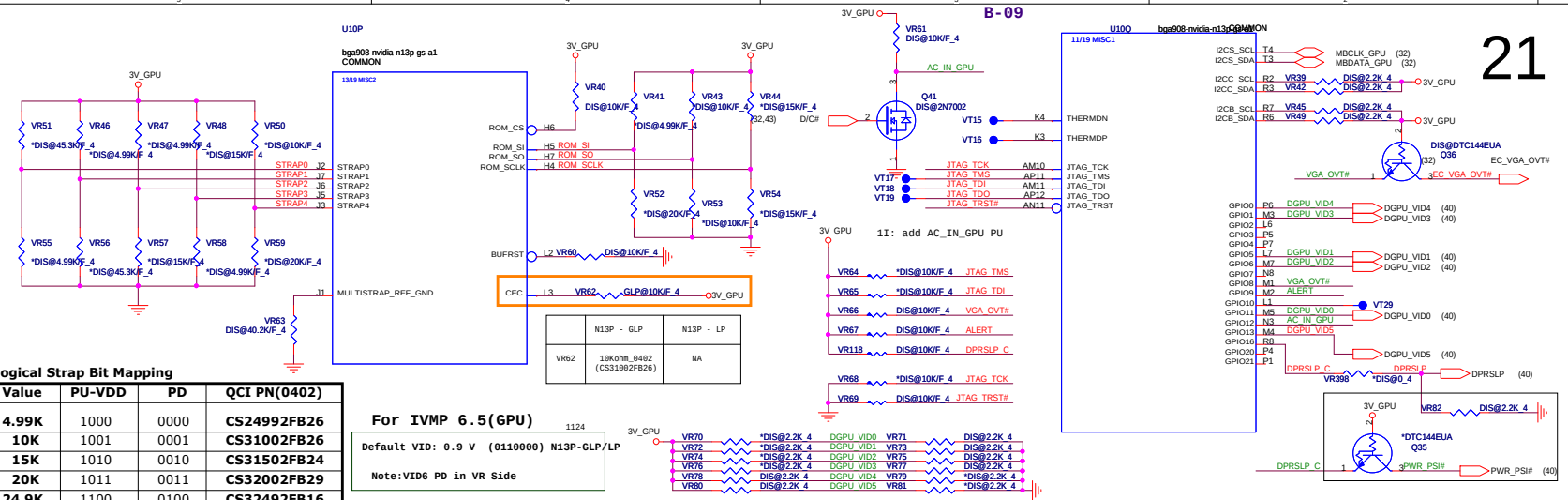
Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	N13P GND	2A
Date: Monday, January 02, 2012	Sheet 20 of 44	



	N13P - GLP	N13P - LP
VR62	10Kohm_0402 (CS31002FB26)	NA

Logical Strap Bit Mapping

Value	PU-VDD	PD	QCI PN(0402)
4.99K	1000	0000	CS24992FB26
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB16
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS33482FB22
45.3K	1111	0111	CS34532FB18

For IVMP 6.5(GPU)

1124

Default VID: 0.9 V (0110000) N13P-GLP/LP

Note:VID6 PD in VR Side

VRAM(DDR3) Configuration Table

RAMCFG [3:0]	DESCRIPTION (Vendor P/N)	Vendor	QCI P/N	ROM_SI
0111	128*16-900MHz K4W2G1646C-HC11	Samsung	AKD5MGWT500	PD 45.3K
0110	128*16-900MHz H5TQ2G63BFR-11C	Hinyx	AKD5MGWTW00	PD 35K
0010	64*16-900MHz H5TQ1G63DFR-11C	Hinyx	AKD5LZWTW02	PD 15K
0011	64*16-900MHz K4W1G1646G-BC11	Samsung	AKD5EGGT500	PD 20K

		GLP 1GB HYN	GLP 1GB SAM	LP 2GB HYN	LP 2GB SAM	GLP 2GB HYN	GLP 2GB SAM
ROM_SCLK	VR44	NA	NA	CS31502FB24	CS31502FB24	NA	NA
	VR54	CS31502FB24	CS31502FB24	NA	NA	CS31502FB24	CS31502FB24
ROM_SI	VR41	NA	NA	NA	NA	NA	NA
	VR52	CS31502FB24	CS32002FB29	CS33482FB22	CS34532FB18	CS33482FB22	CS34532FB18
ROM_SO	VR43	NA	NA	NA	NA	NA	NA
	VR53	CS31002FB26	CS31002FB26	CS33012FB18	CS31002FB26	CS31002FB26	CS31002FB26
STRAP0	VR51	CS34532FB18	CS34532FB18	CS34532FB18	CS34532FB18	CS34532FB18	CS34532FB18
	VR55	NA	NA	NA	NA	NA	NA
STRAP1	VR46	NA	NA	NA	NA	NA	NA
	VR56	CS34532FB18	CS34532FB18	CS33482FB22	CS33482FB22	CS34532FB18	CS34532FB18
STRAP2	VR47	CS24992FB26	CS24992FB26	CS33482FB22	CS33482FB22	CS24992FB26	CS24992FB26
	VR57	NA	NA	NA	NA	NA	NA
STRAP3	VR48	NA	NA	NA	NA	NA	NA
	VR58	CS24992FB26	CS24992FB26	CS24992FB26	CS24992FB26	CS24992FB26	CS24992FB26
STRAP4	VR50	NA	NA	NA	NA	NA	NA
	VR59	NA	NA	CS34532FB18	CS34532FB18	NA	NA

N13P-LP	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	Value	Note
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG-GLP	PEX_PLL_EN_TERM	1000	LP:ES Samples 5K PU(0X0FDB)
			PCI_DEVIDE[5]-LP		0010	GLP:ES Samples 15K PD(0X0DFE)
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0110	LP K4W2G1646C-HC11 45.3K PD
					0111	LP H5TQ2G63BFR-11C :35K PD
					0010	GLP H5TQ1G63DFR-11C :15K PD
					0011	GLP K4W1G1646G-BC11 :20K PD
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	1001	10K PU
	FB[1]-LP	FB[0]-LP	I2CS ADDR:0X9E		0001	10K PD
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111	EDID is used :45K PU
					0110	LP:notebook default:35K PD
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0111	GLP: Reserve:45.3K PD
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0011	ES Samples LP:20K PU(0X0FDB)
					1000	ES Samples GLP:45.3K PU(0X0DEF)
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000	Not in use :5K PD
STRAP4	RESERVED	Reserve PCIE_SPEED-LP	PCIE_MAX_SPEED	DP_PLL_VDD3V	0001	LP:10K PD GLP: NA

*LP QS Samples :5K PD(0X0FD3)

GLP:MP Samples:15K PD(0X0DE8)

*LP QS Samples : 20K PU(0X0FD3)

*GLP:MP Samples :5K PU(0X0DE8)

GPIO ASSIGNMENTS

GPIO	I/O	USAGE	
0	OUT	Y	NVVDD VID4
1	OUT	Y	NVVDD VID3
2	OUT	N	PANEL BACKLIGHT PWM
3	OUT	N	PANEL POWER ENABLE
4	OUT	N	PANEL BACKLIGHT ENABLE
5	OUT	Y	NVVDD VID1
6	OUT	Y	NVVDD VID2
7	OUT	N	3D STEREO
8	I/O	Y	GPU Overtemp
9	I/O	Y	GPU ALERT
10	OUT	N	FB Vref Control
11	OUT	Y	NVVDD VID0
12	IN	N	PWR_Level AC Detect
13	OUT	Y	NVVDD VID5
14	IN	N	HPD for IFP AB
15	IN	N	HPD for IFP C
16	OUT	N	MEM_VDD_CTL
17	OUT	N	HPD for IFP D
18	OUT	N	HPD for IFP E
19	OUT	N	HPD for IFP F
20	OUT	N	
21	OUT	N	

Quanta Computer Inc.
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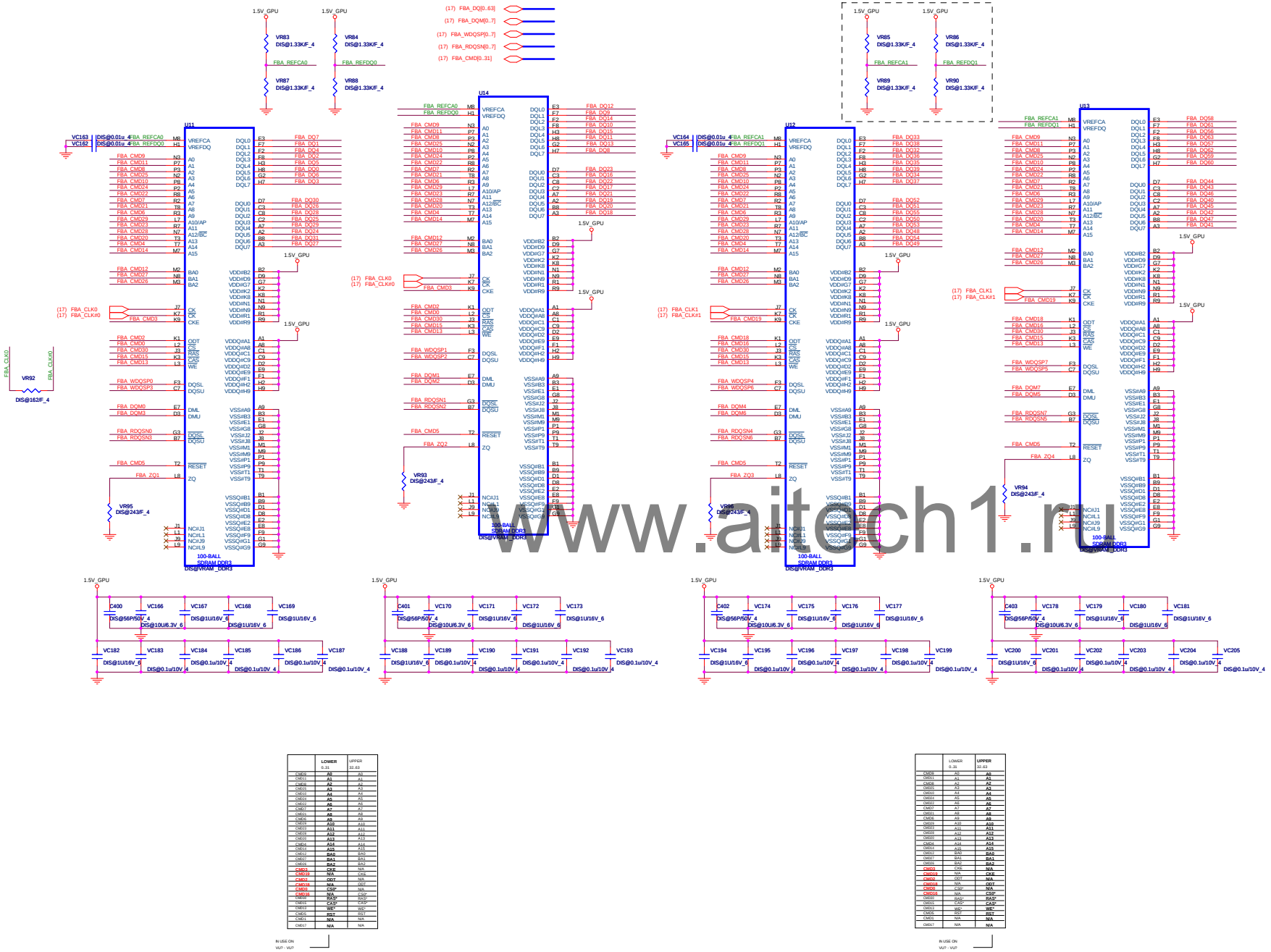
Size	Document Number	Rev
	N13P STRAP/GPIO	2A
Date: Monday, January 02, 2012	Sheet 21 of 44	

SAM : AKD5EGGT500
HYU : AKD5LZWTW02



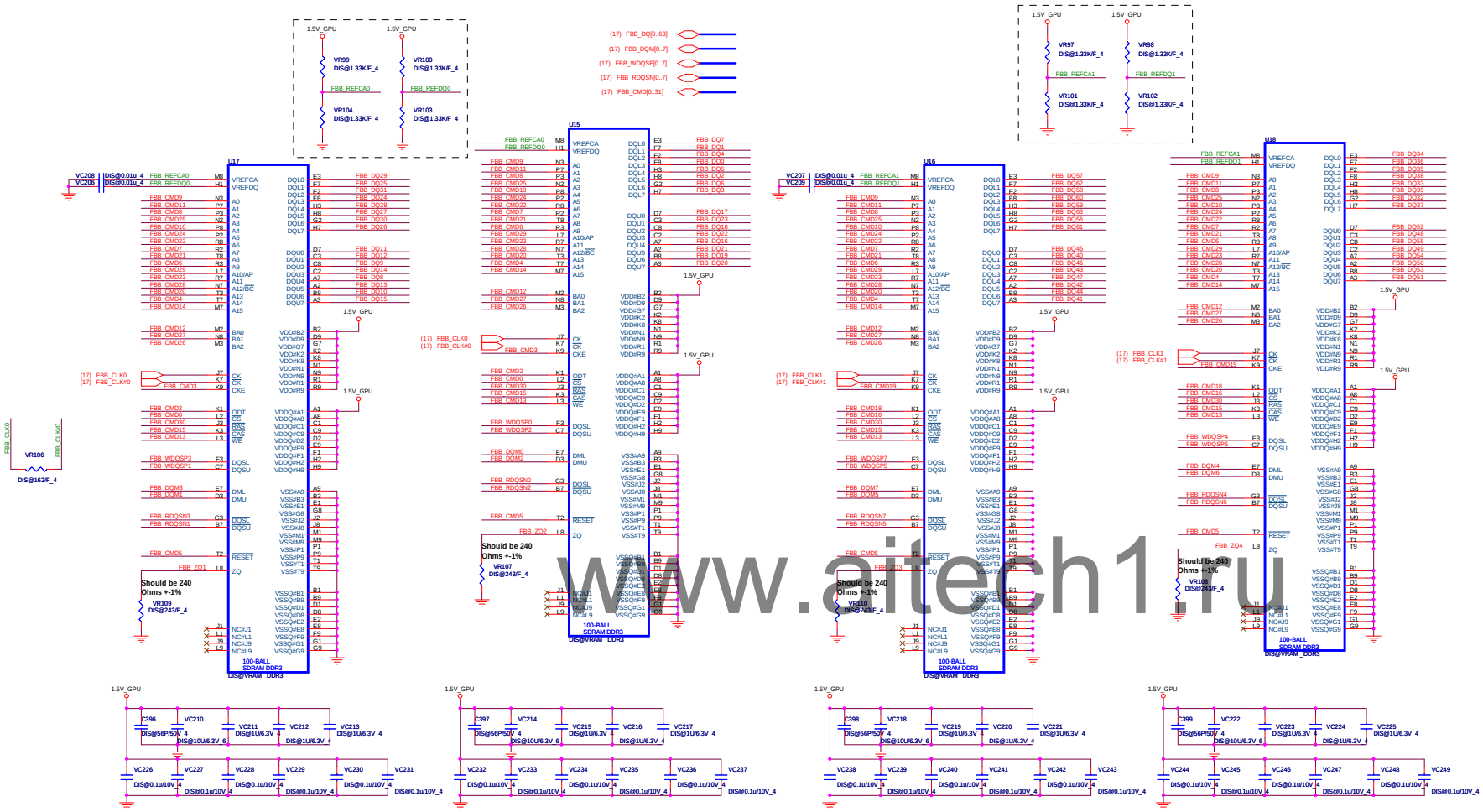
	LOWER 0..31	UPPER 32..63
CMD0	A0	A0
CMD1	A1	A1
CMD2	A2	A2
CMD3	A3	A3
CMD4	A4	A4
CMD5	A5	A5
CMD6	A6	A6
CMD7	A7	A7
CMD8	A8	A8
CMD9	A9	A9
CMD10	A10	A10
CMD11	A11	A11
CMD12	A12	A12
CMD13	A13	A13
CMD14	A14	A14
CMD15	A15	A15
CMD16	BA0	BA0
CMD17	BA1	BA1
CMD18	BA2	BA2
CMD19	CKE	N/A
CMD20	ODT	N/A
CMD21	N/A	ODT
CMD22	CS*	N/A
CMD23	RAS*	CS*
CMD24	CAS*	RAS*
CMD25	WE*	CAS*
CMD26	RST	WE*
CMD27	N/A	RST
CMD28	N/A	N/A

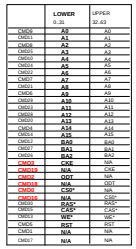
IN USE ON
VU7 - VU7

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FJ8
Size: Document Number: N13P VRAM-A DDR3 Rev: 2A
Date: Monday, January 02, 2012 Sheet 22 of 44

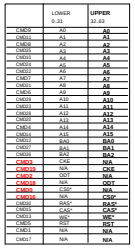
SAM : AKD5EGGT500
HYU : AKD5LZWTW02





	LOWER 0..31	UPPER 32..63
CMD0	A0	A0
CMD1	A1	A1
CMD2	A2	A2
CMD3	A3	A3
CMD4	A4	A4
CMD5	A5	A5
CMD6	A6	A6
CMD7	A7	A7
CMD8	A8	A8
CMD9	A9	A9
CMD10	A10	A10
CMD11	A11	A11
CMD12	A12	A12
CMD13	A13	A13
CMD14	A14	A14
CMD15	A15	A15
CMD16	BA0	BA0
CMD17	BA1	BA1
CMD18	BA2	BA2
CMD19	CKE	N/A
CMD20	ODT	N/A
CMD21	N/A	ODT
CMD22	CS#	N/A
CMD23	RAS#	CS#
CMD24	CAS#	RAS#
CMD25	WE#	CAS#
CMD26	RST	WE#
CMD27	N/A	RST
CMD31	N/A	N/A

IN USE ON VU7 - VU7



	LOWER 0..31	UPPER 32..63
CMD0	A0	A0
CMD1	A1	A1
CMD2	A2	A2
CMD3	A3	A3
CMD4	A4	A4
CMD5	A5	A5
CMD6	A6	A6
CMD7	A7	A7
CMD8	A8	A8
CMD9	A9	A9
CMD10	A10	A10
CMD11	A11	A11
CMD12	A12	A12
CMD13	A13	A13
CMD14	A14	A14
CMD15	A15	A15
CMD16	BA0	BA0
CMD17	BA1	BA1
CMD18	BA2	BA2
CMD19	CKE	N/A
CMD20	ODT	N/A
CMD21	N/A	ODT
CMD22	CS#	N/A
CMD23	RAS#	CS#
CMD24	CAS#	RAS#
CMD25	WE#	CAS#
CMD26	RST	WE#
CMD27	N/A	RST
CMD31	N/A	N/A

IN USE ON VU7 - VU7

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	N13P VRAM-B DDR3	2A
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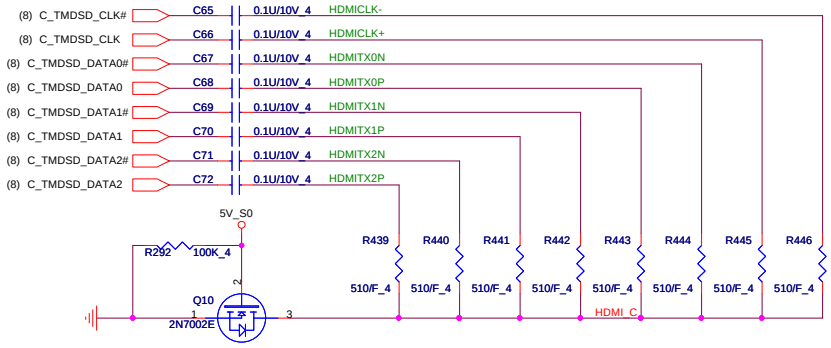
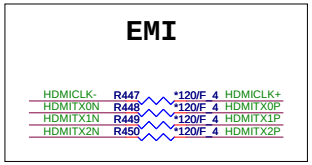
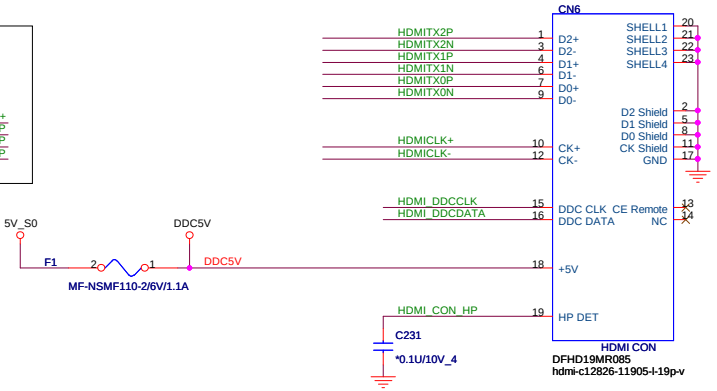


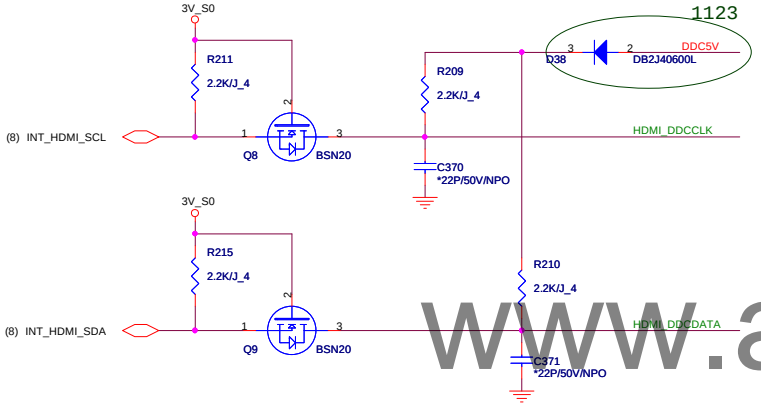
EMI



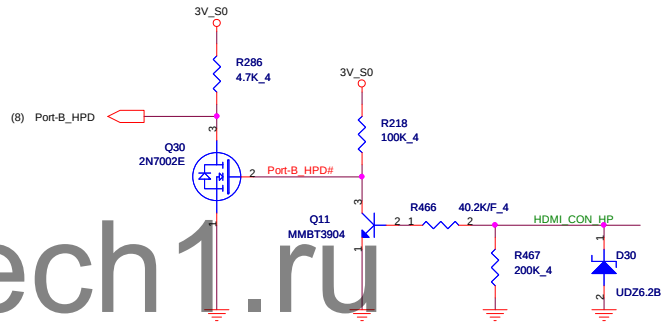
HDMI Conn



DDC Level Shift

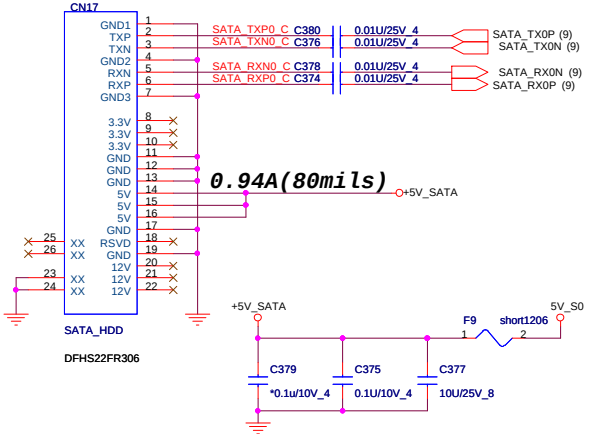


HPD

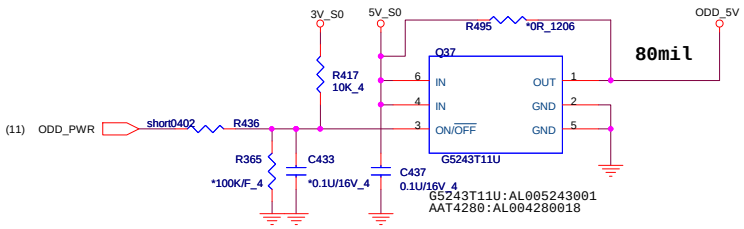


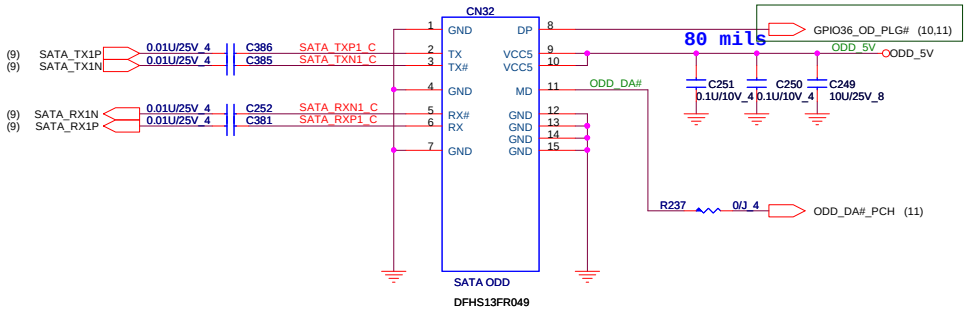
2.5" SATA HDD

DFHS22FR306
DFHS22FR282



SATA ODD





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	DMI/HDD/ODD	2A
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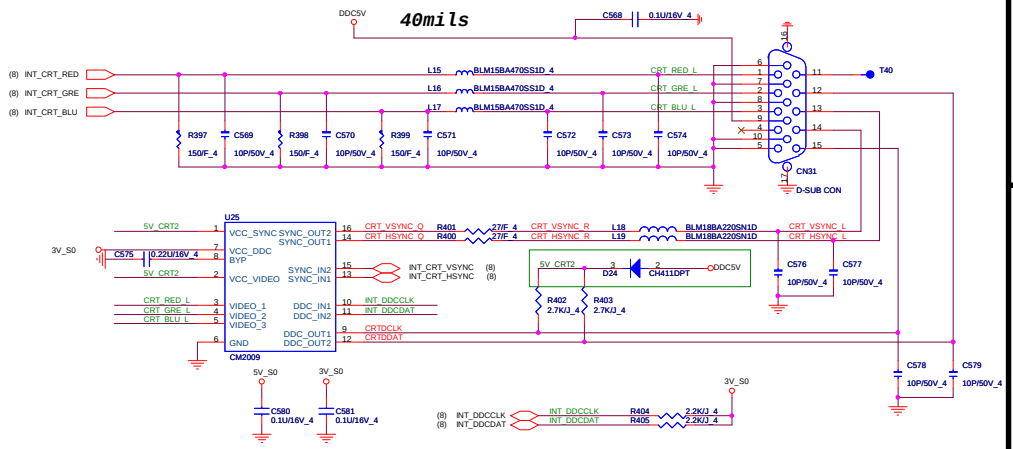
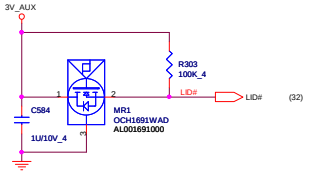
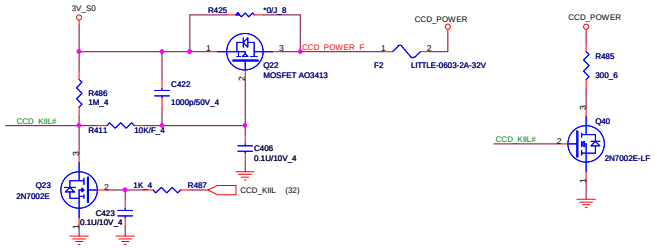
CRT CONN/DDC LEVEL SHIFT



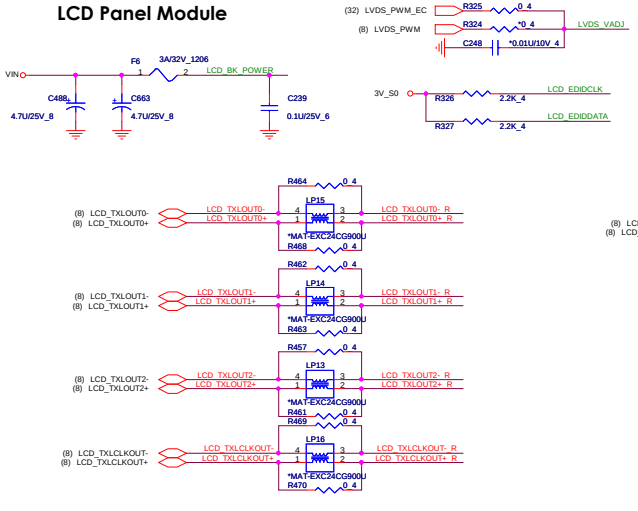
HALL SENSOR

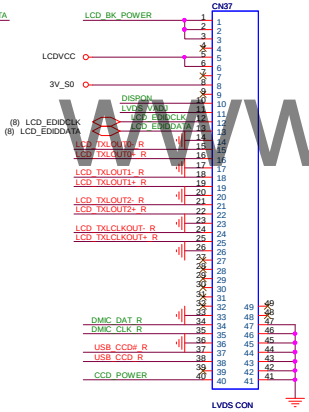


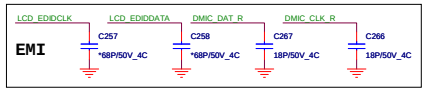
CCD KILL



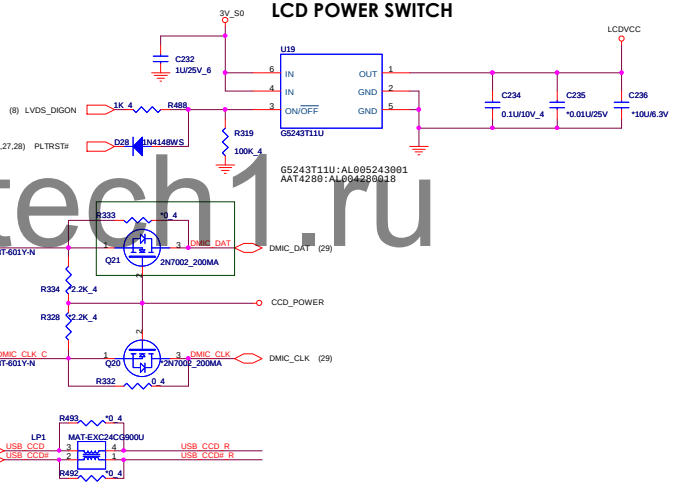
LCD Panel Module



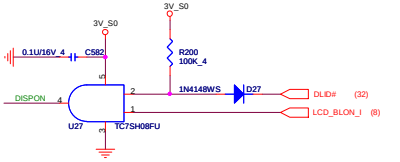




LCD POWER SWITCH



PANEL BACKLIGHT CONTROL



Quanta Computer Inc.
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Size	Document Number	Rev
	LVDS/CCD/CRT	2A

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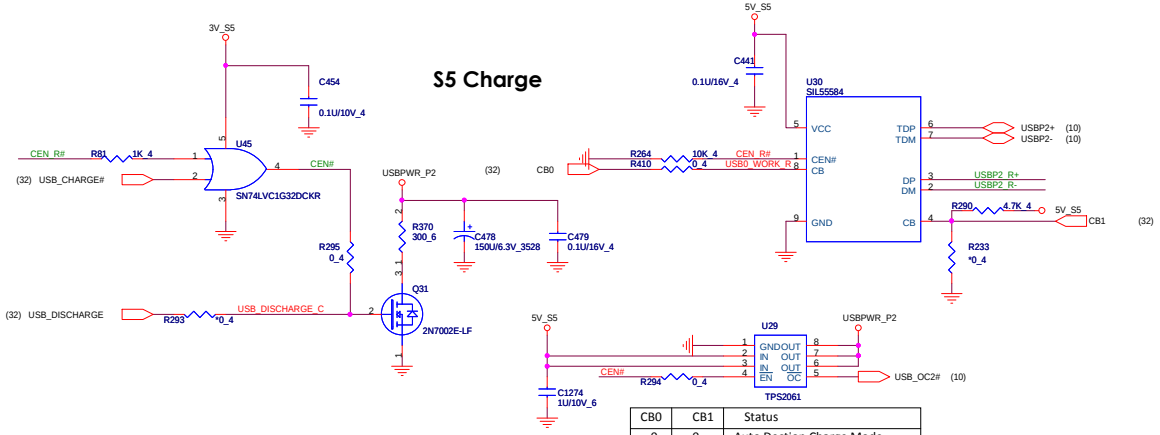
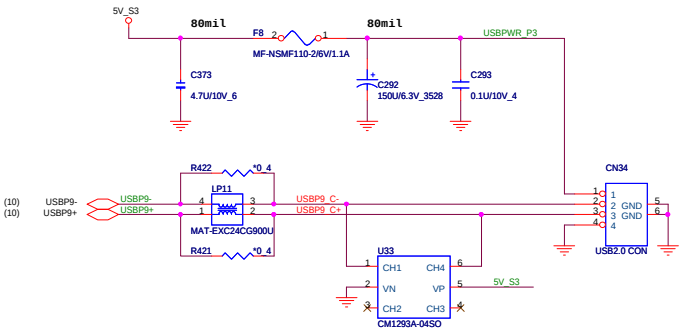
S5 Charge



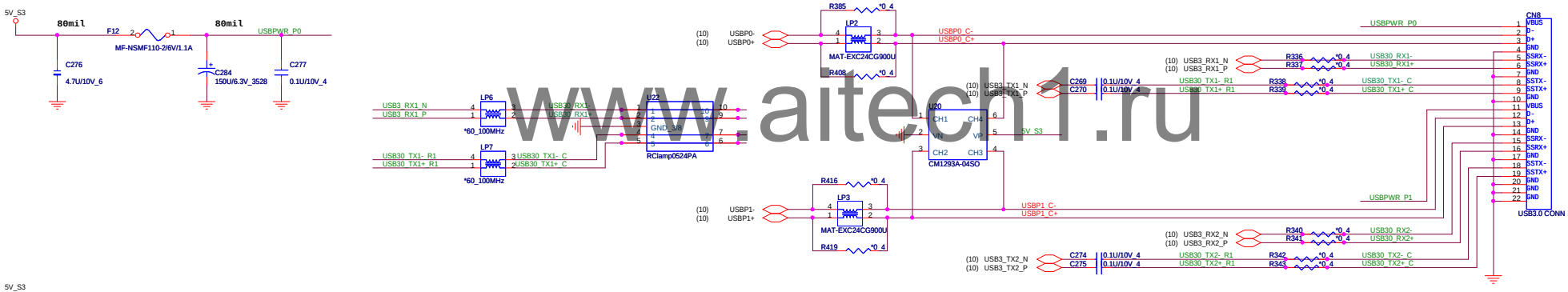
CB0	CB1	Status
0	0	Auto Dection Charge Mode
0	1	Force Dedicated Charger Mode
1	0	Pass Through Mode
1	1	Pass Through Mode with CDP

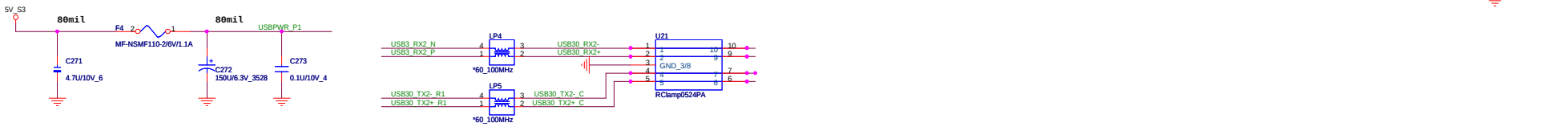
USB 2.0 CONN



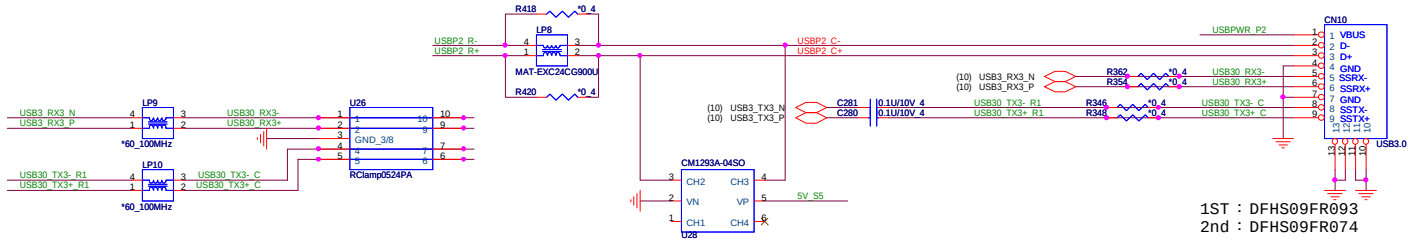
USB 3.0 CONN

SIT : DFHS18FR021
FOX : DFHS18FR019





USB 3.0 CONN (S5 Charge)



1ST : DFHS09FR093
2nd : DFHS09FR074

Quanta Computer Inc.
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Size	Document Number	Rev
	USB 3.0/USB 2.0	2A
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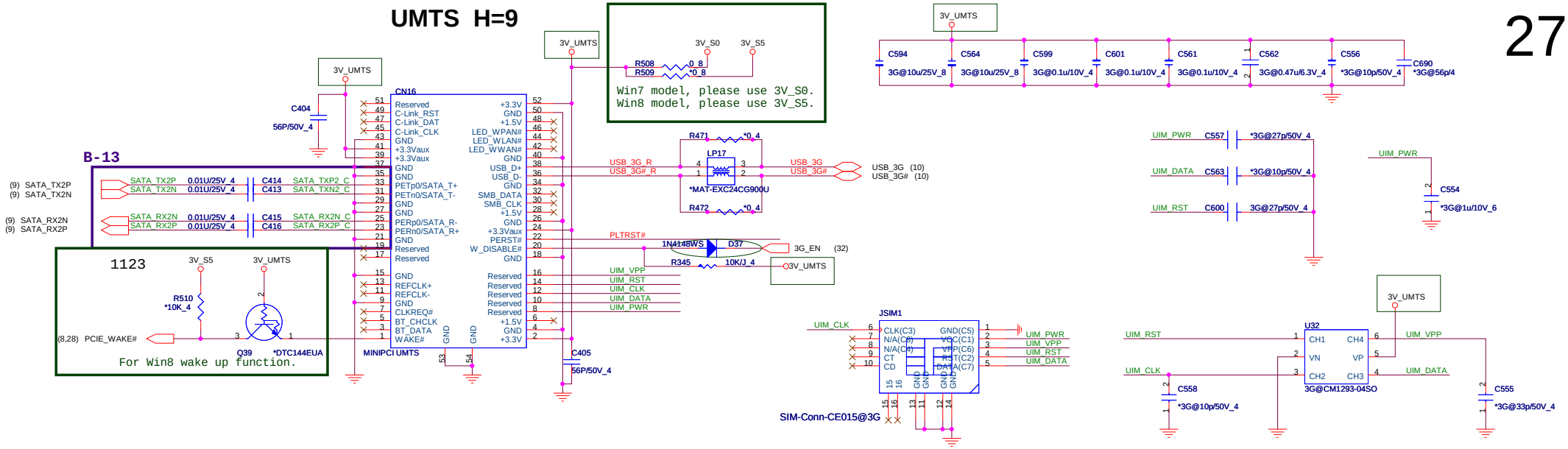
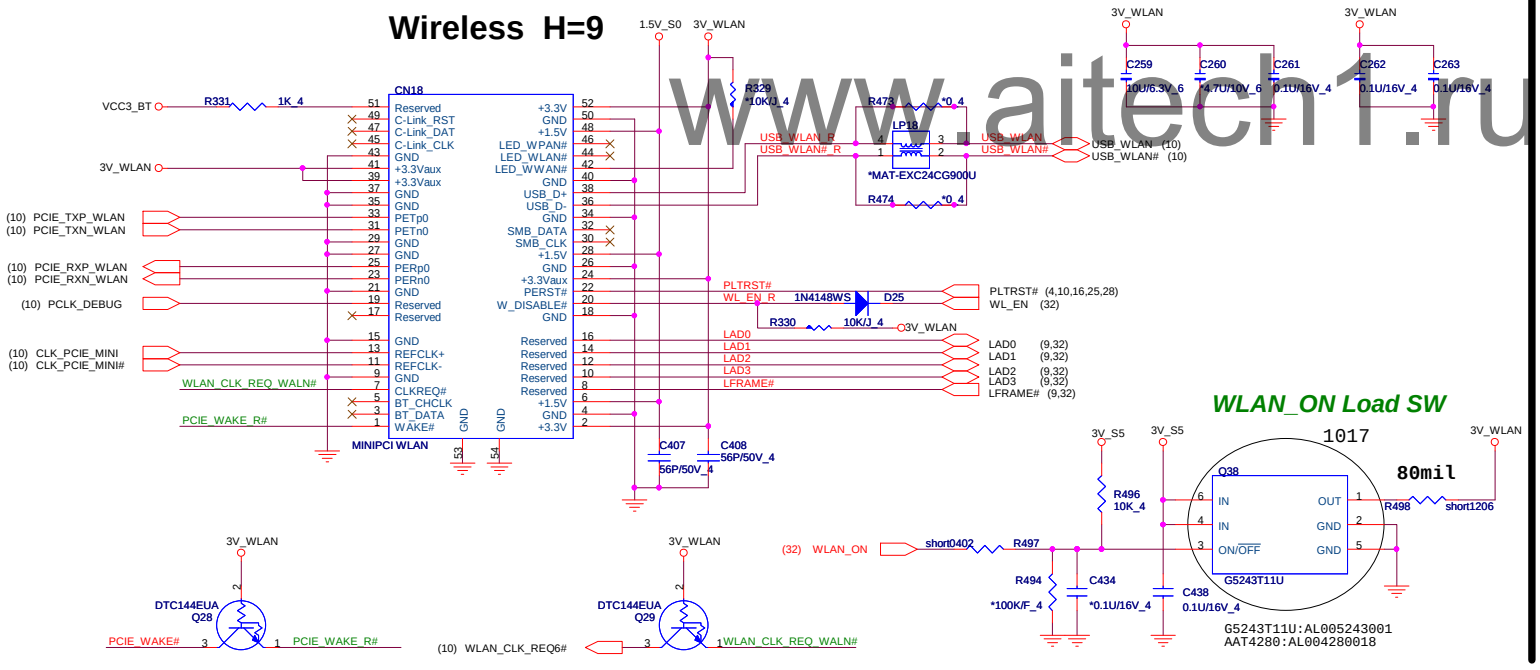
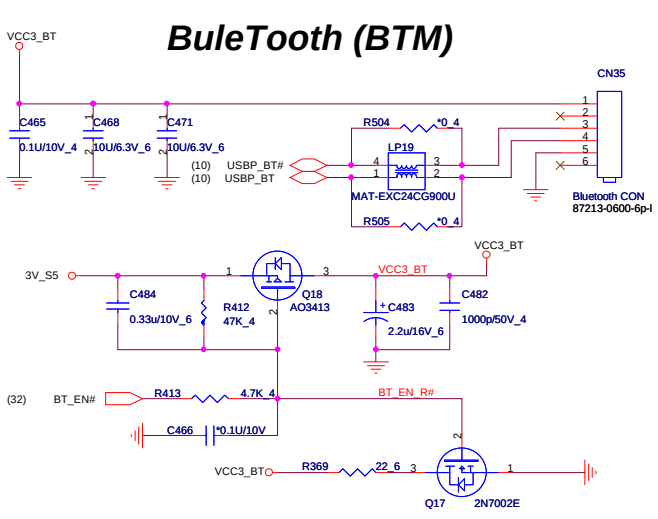
UMTS H=9



Wireless H=9

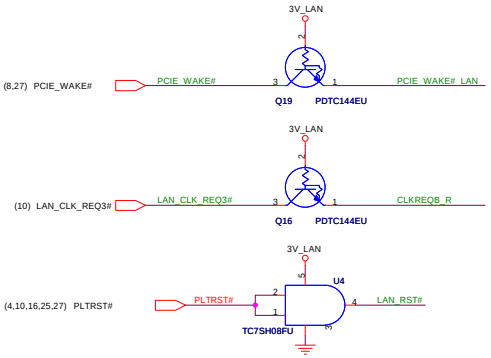


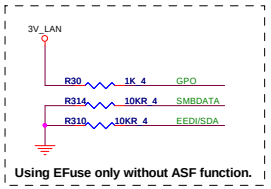
BuleTooth (BTM)

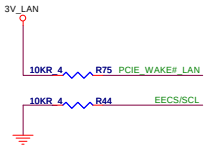


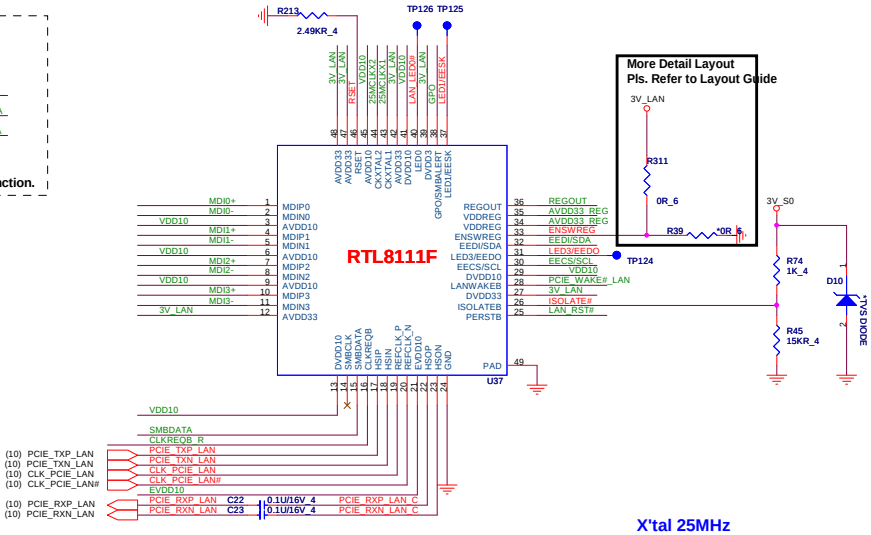
Quanta Computer Inc.
PROJECT : FJ8

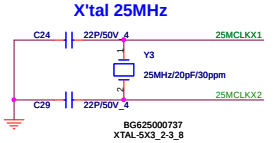
Size	Document Number	Rev
	WLAN/UMTS/BT	2A
Date: Monday, January 02, 2012	Sheet 27 of 44	

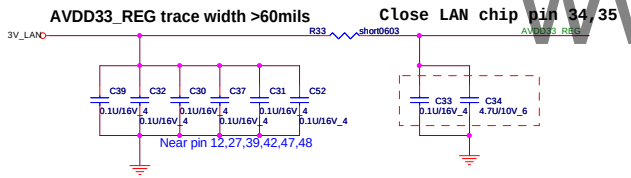


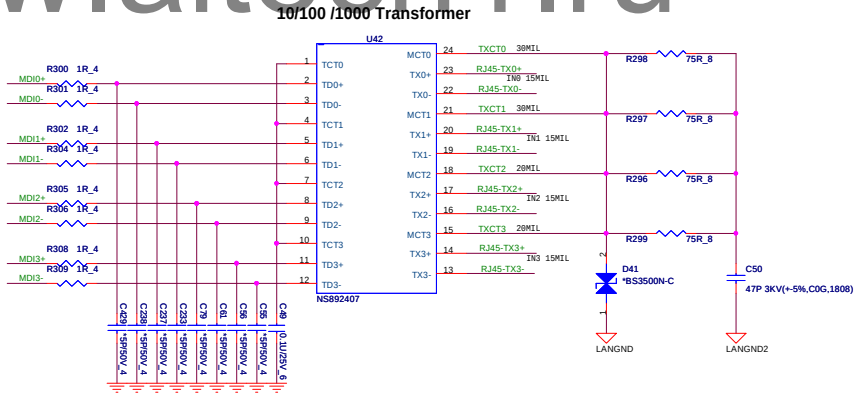


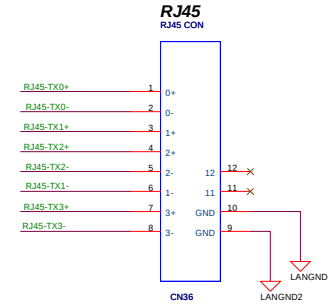


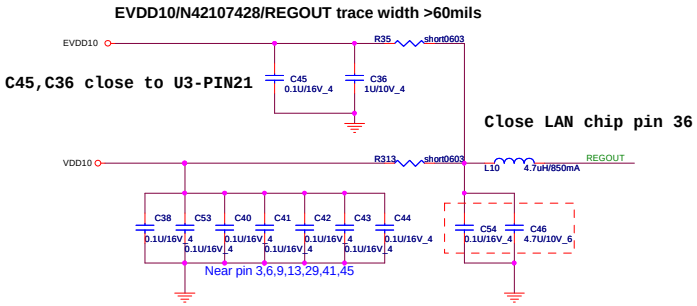


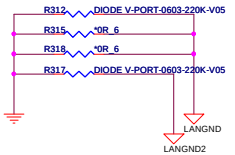












Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	LAN RTL8111F	1A
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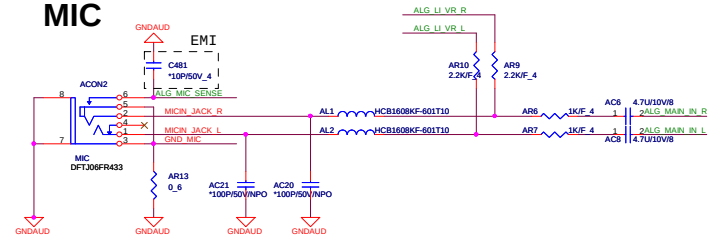
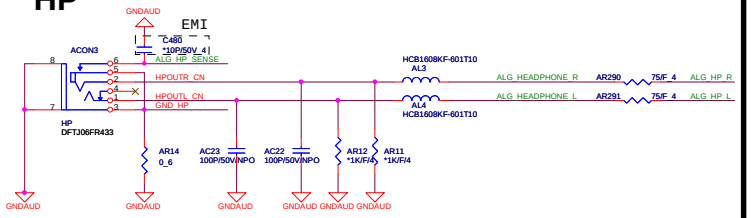
Codec ALC269-VC3

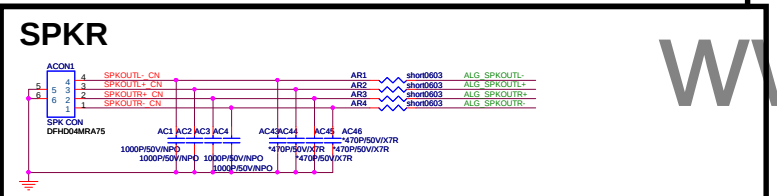
MIC



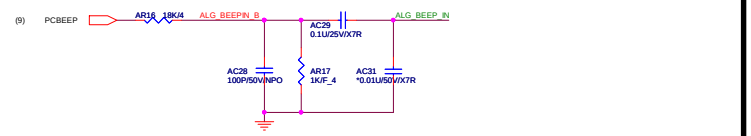
HP



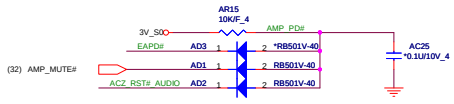
SPKR

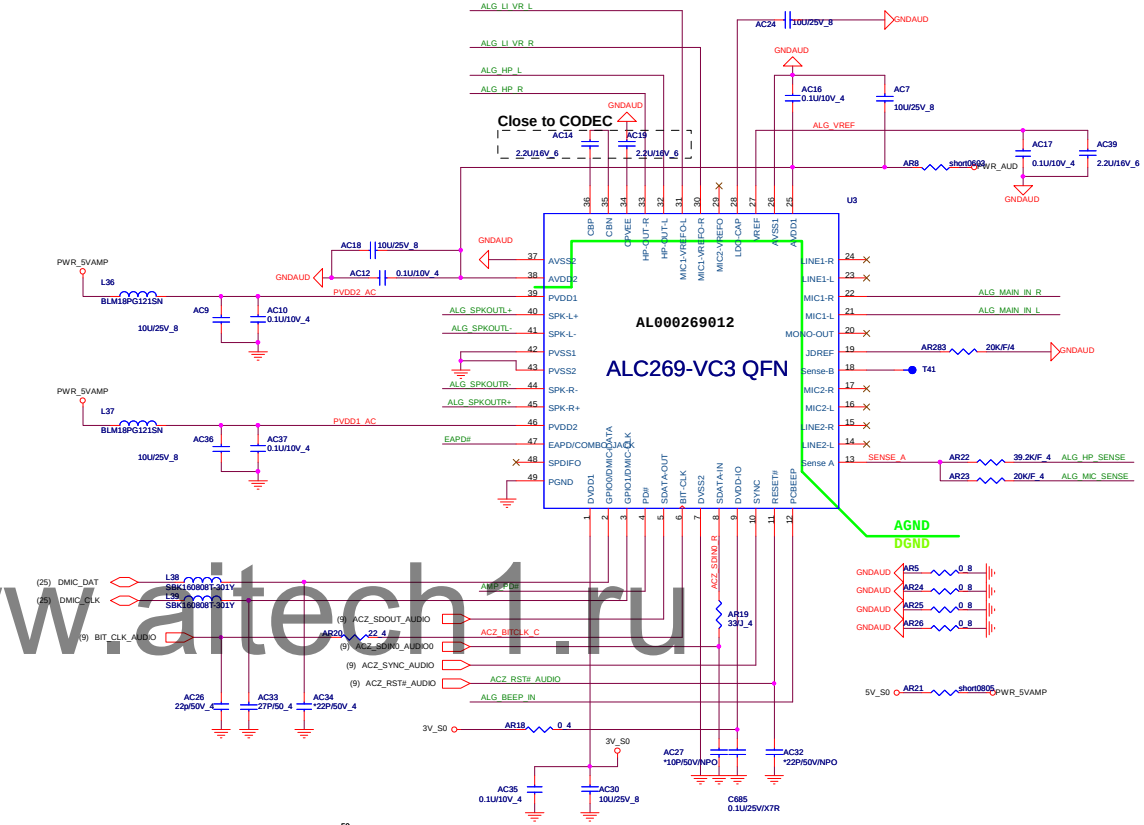


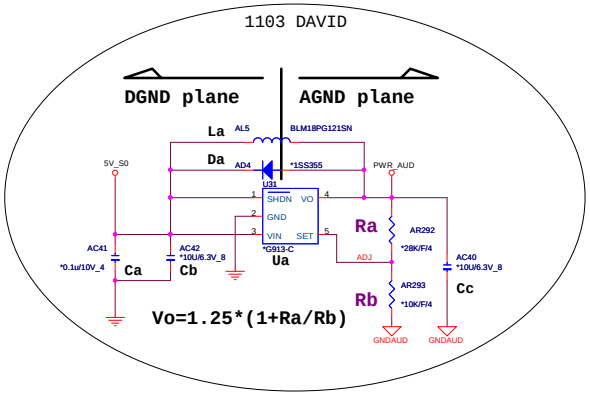
BEEP



VOLMUTE







Quanta Computer Inc.		
PROJECT : FJ8		
Size	Document Number	Rev
	CODEC (ALC269Q-VC3)	2A
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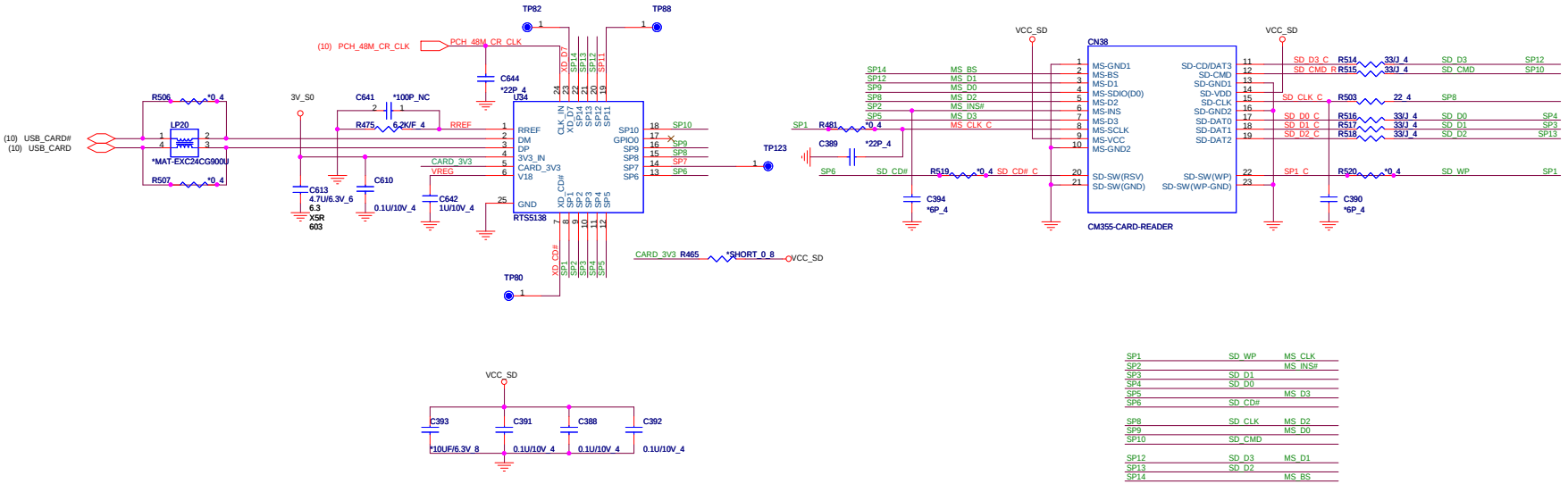
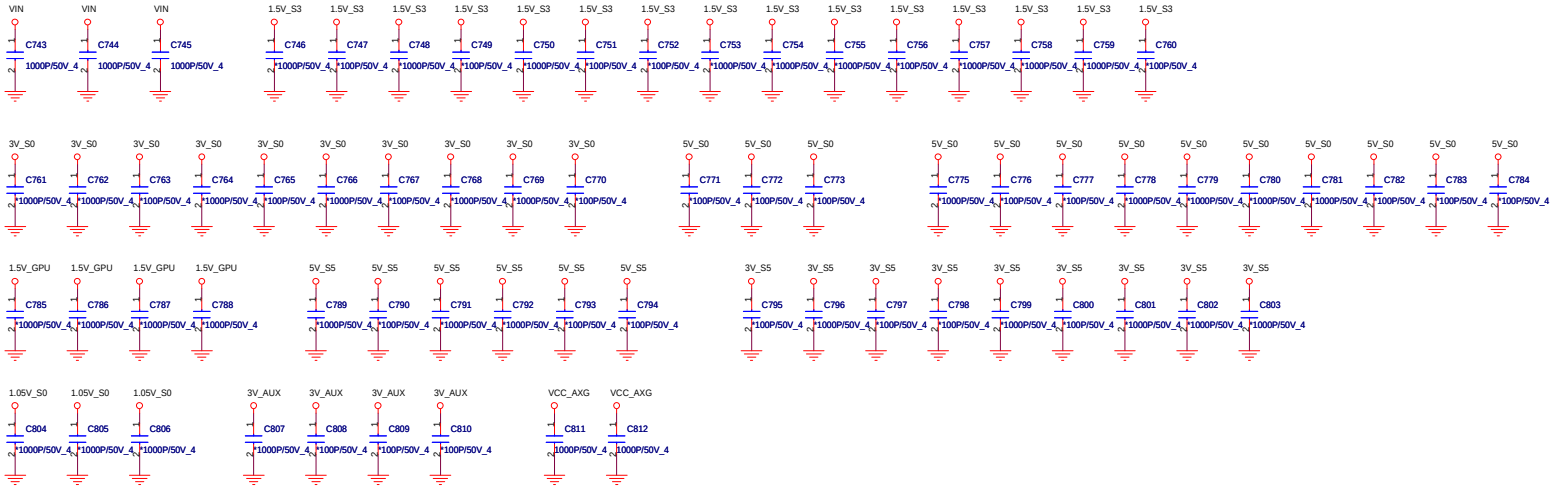


SP1	SD_WP	MS_CLK
SP2		MS_INS#
SP3	SD_D1	
SP4	SD_D0	
SP5		MS_D3
SP6	SD_CD#	
SP8	SD_CLK	MS_D2
SP9		MS_D0
SP10	SD_CMD	
SP12	SD_D3	MS_D1
SP13	SD_D2	
SP14		MS_BS



Quanta Computer Inc.
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Size	Document Number	Rev
	NEW CARD/CARD READER	2A
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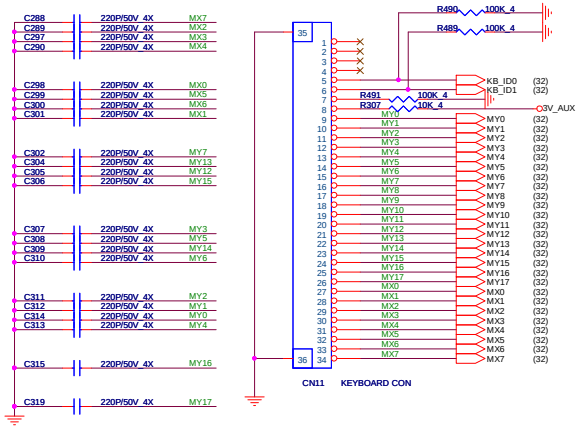
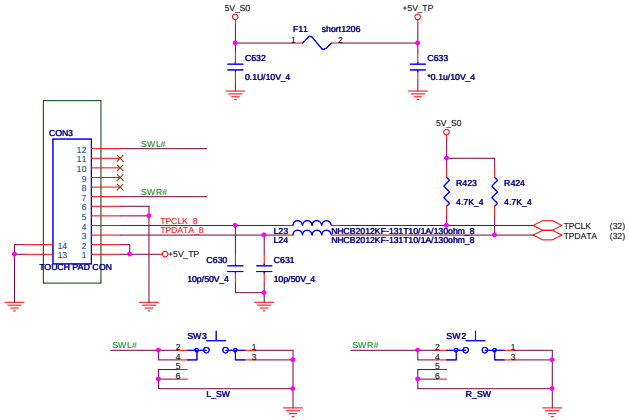
INT KeyBoard

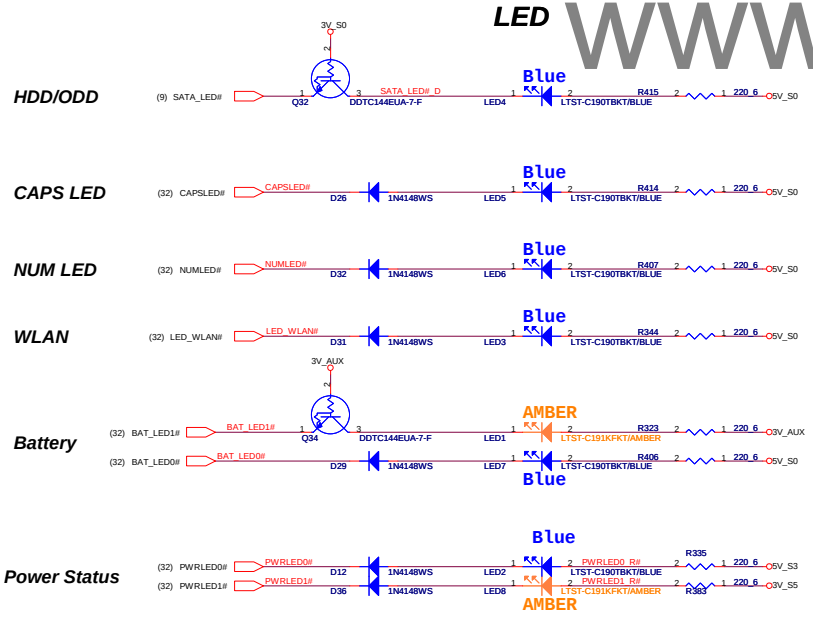


	R490 ID0	R489 ID1	R491 ID2	R307 KB_ID
UK	1	0	0	1
US	0	1	0	1
JP	1	1	0	1

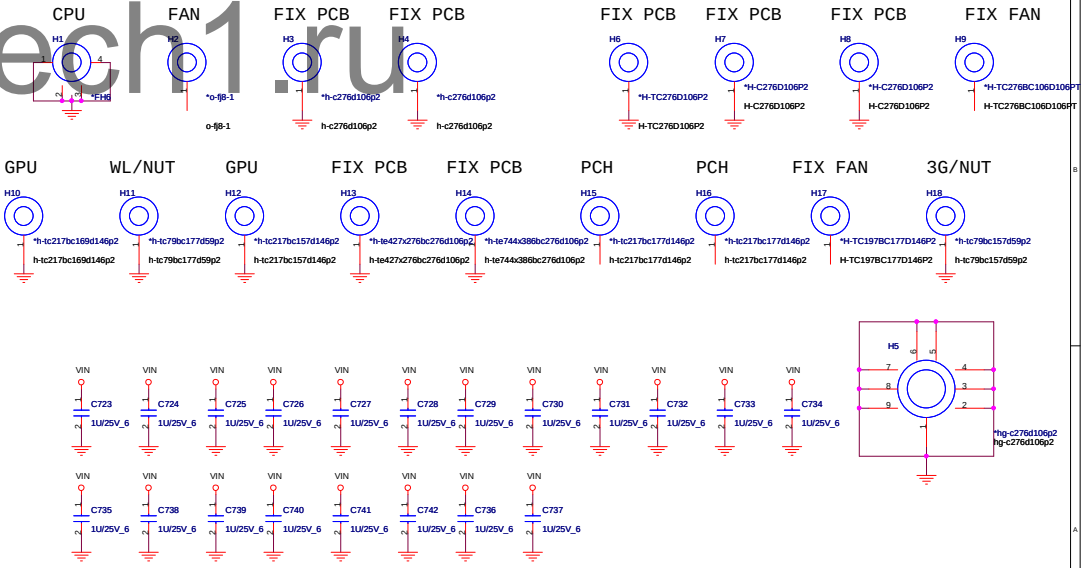
Touch Pad



LED



HOLE



Quanta Computer Inc.
PROJECT : FJ8
Size | Document Number: TPM/KB/TP/LED/HOLE | Rev 2A
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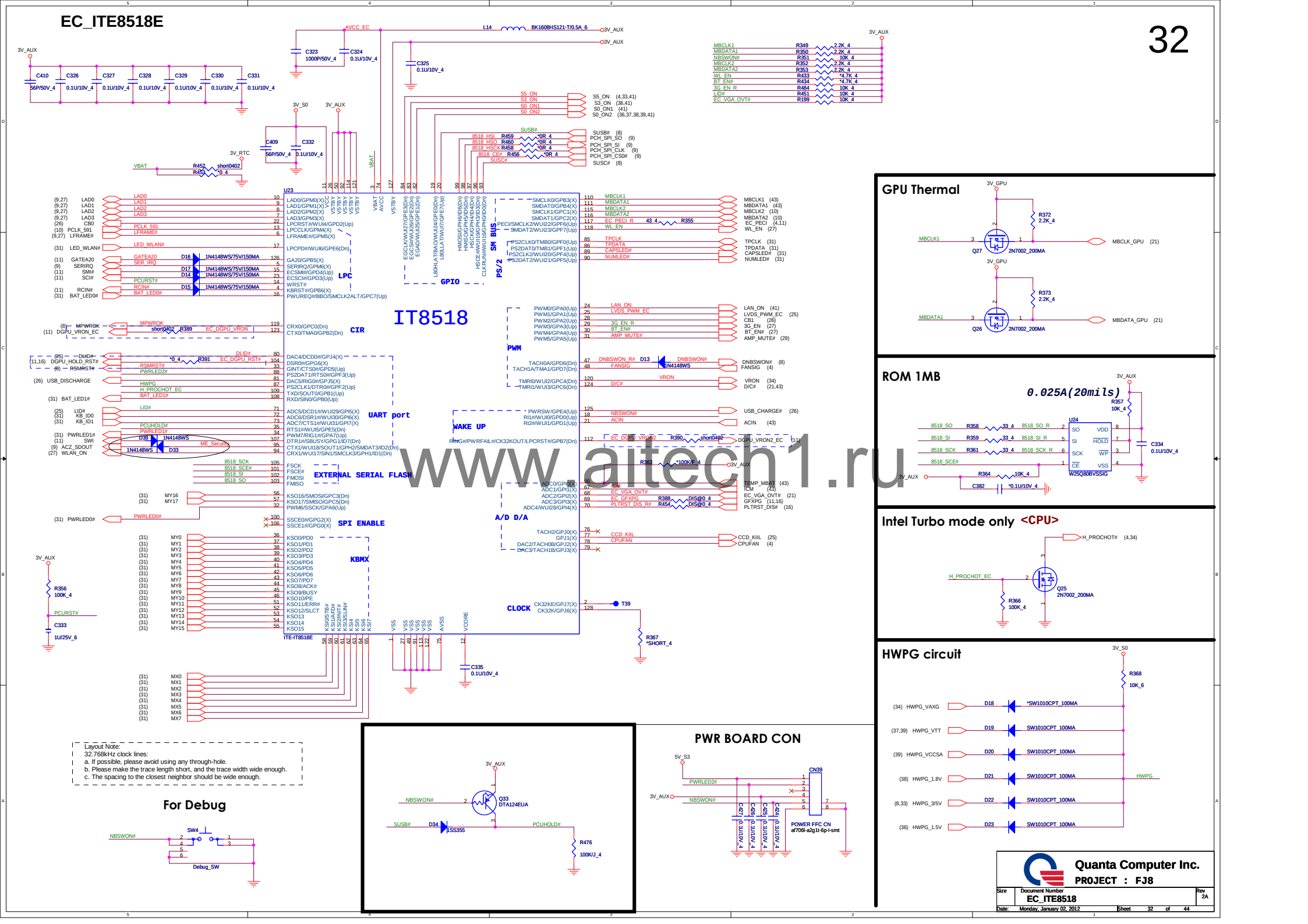
EC_ITE8518E



GPU Thermal

ROM 1MB

Intel Turbo mode only <CPU>

HWPG circuit

PWR BOARD CON

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

For Debug

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	EC_ITE8518	2A
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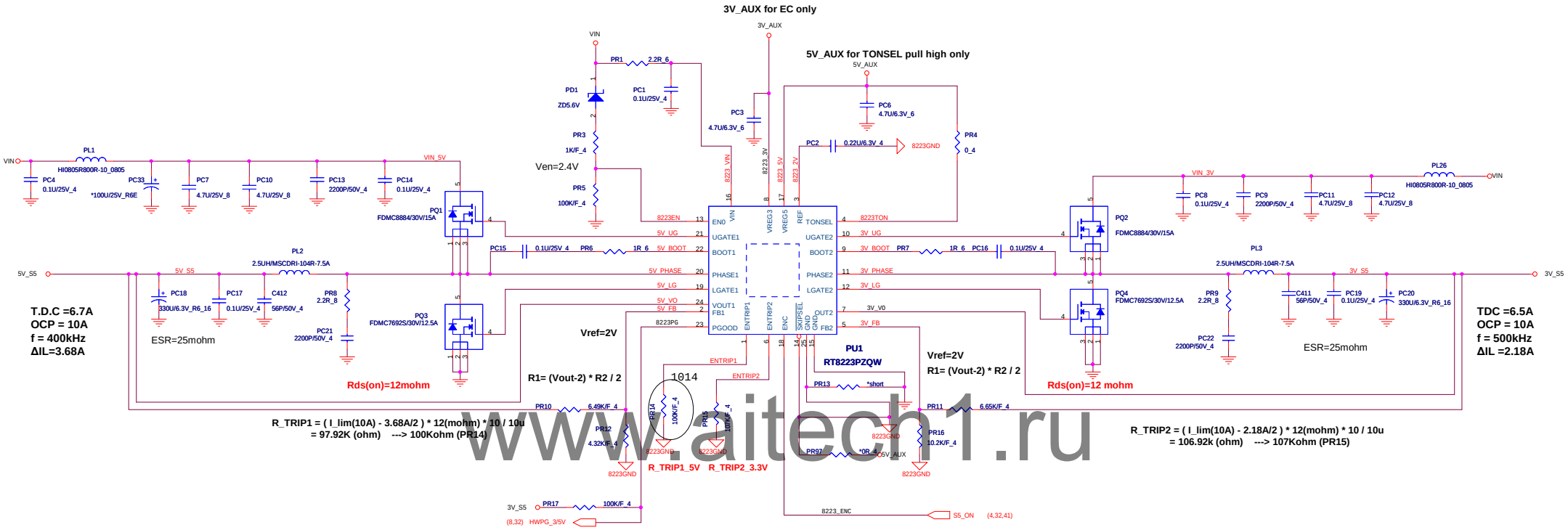
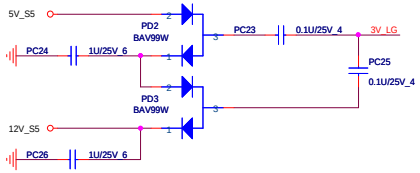
System 3V_S5 and 5V_S5 (RT8223PZQW)





Iripple=(Vin-Vout)*Vout/(Vin*L*f)

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
5V	17.5m_Max	10	3.68	400	2.5uH	100K
3.3V	17.5m_Max	10	2.18	500	2.5uH	107K

L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max
Si4134DY	SO-8	9.9A/14A	17.5m
AO4712	SO-8	10A/11.2A	18.0m
AO4710	SO-8	11A/12.7A	14.2m
AP4438GSM	SO-8	7A/11.7A	18.0m
DMG4812	SO-8	9.6A/10.7A	18.5m
AON7702	DFN3x3	11A/20A	14.0m
FDMC7692S	DFN3x3	12A/30A	12.0m

Power On sequencing

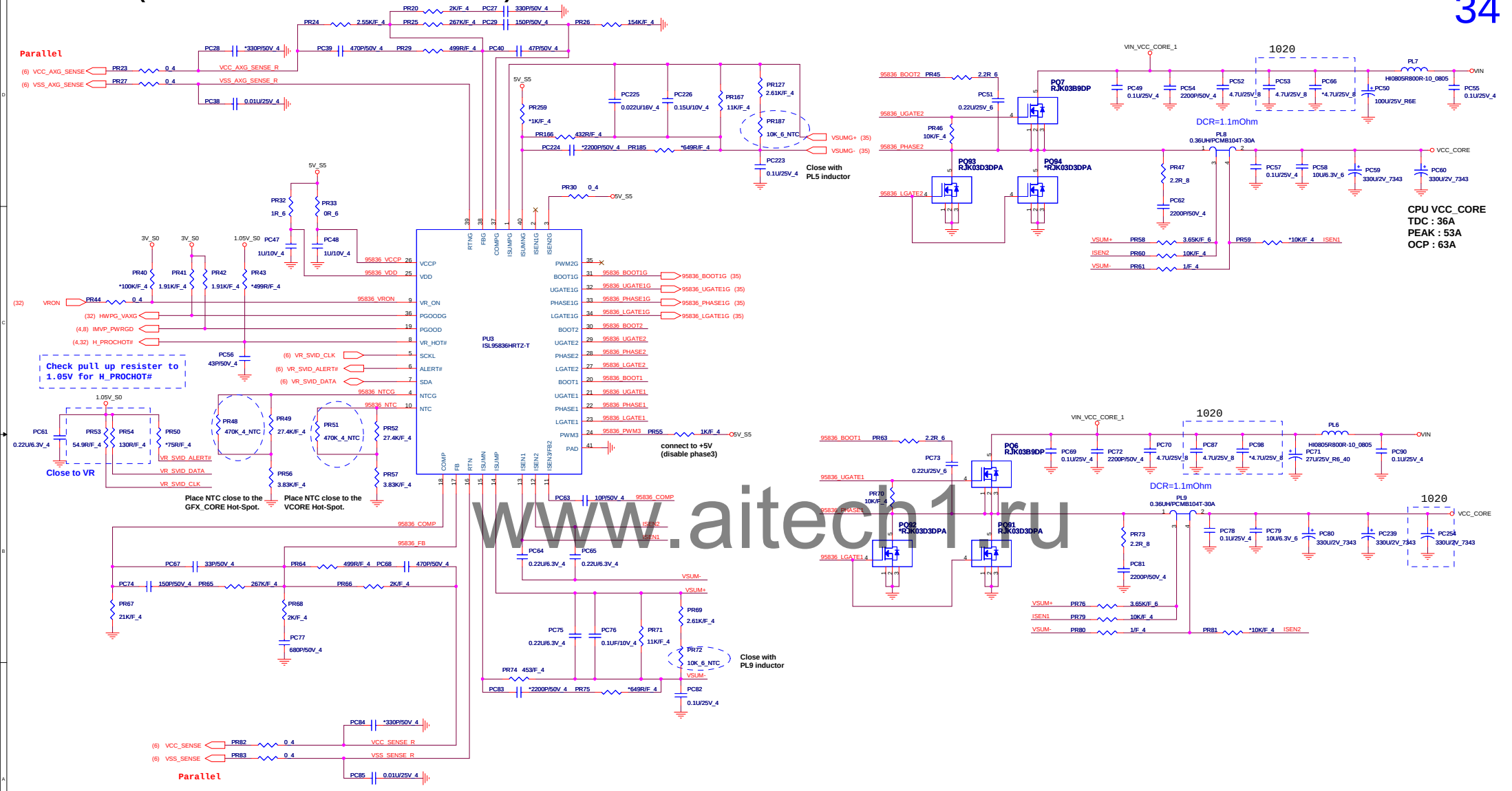
EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	System 3V_S5 and 5V_S5 (RT8223PZQW)	2A

Date: Monday, January 02, 2012 Sheet 33 of 44

CPU VCORE (ISL95836HRTZ-T and ISL6208CRZ-T)

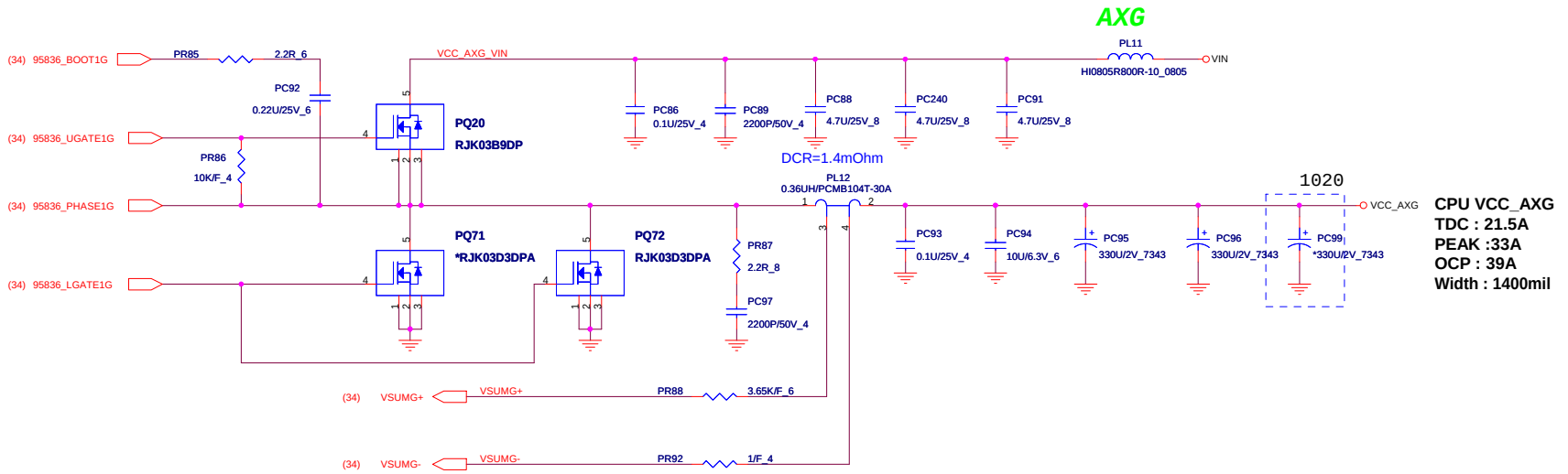


Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size	Vendor P/N
0.36uH 20%	CYN	CV+36V0MZ13	30	50	1.4m Max.	10x10x4	PCMB104T-R36MT
0.36uH 20%	Panasonic	CV+18V0MZ04	30	34	1.4m Max.	10x10x4	ETQP4LR36WFC

Quanta Computer Inc.
PROJECT : FJ8
Size | Document Number: CPU_CORE (ISL95836HRTZ-T and ISL6208CRZ-T) | Rev: 2A
Date: Monday, January 02, 2012 | Sheet 34 of 44

VCC_AXG (ISL95836HRTZ-T)



CPU VCC_AXG
TDC : 21.5A
PEAK :33A
OCP : 39A
Width : 1400mil

Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size	Vendor P/N
0.36uH 20%	Panasonic	CV+36Q0MZ00	20	25	1.4m Max.	7X7X4	ETQP4LR36AFM

L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
RJK03D3DPA	P_PAK	20A/40A	4.7m	YES
AOL1718	P_PAK	20A/90A	4.3m	YES
RMW200N03FUB	P_PAK	20A/80A	4.6m	NO
FDMS0310S	P_PAK	14A/83A	5.2m	YES

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	CPU_GFX (ISL95836HRTZ-T)	2A

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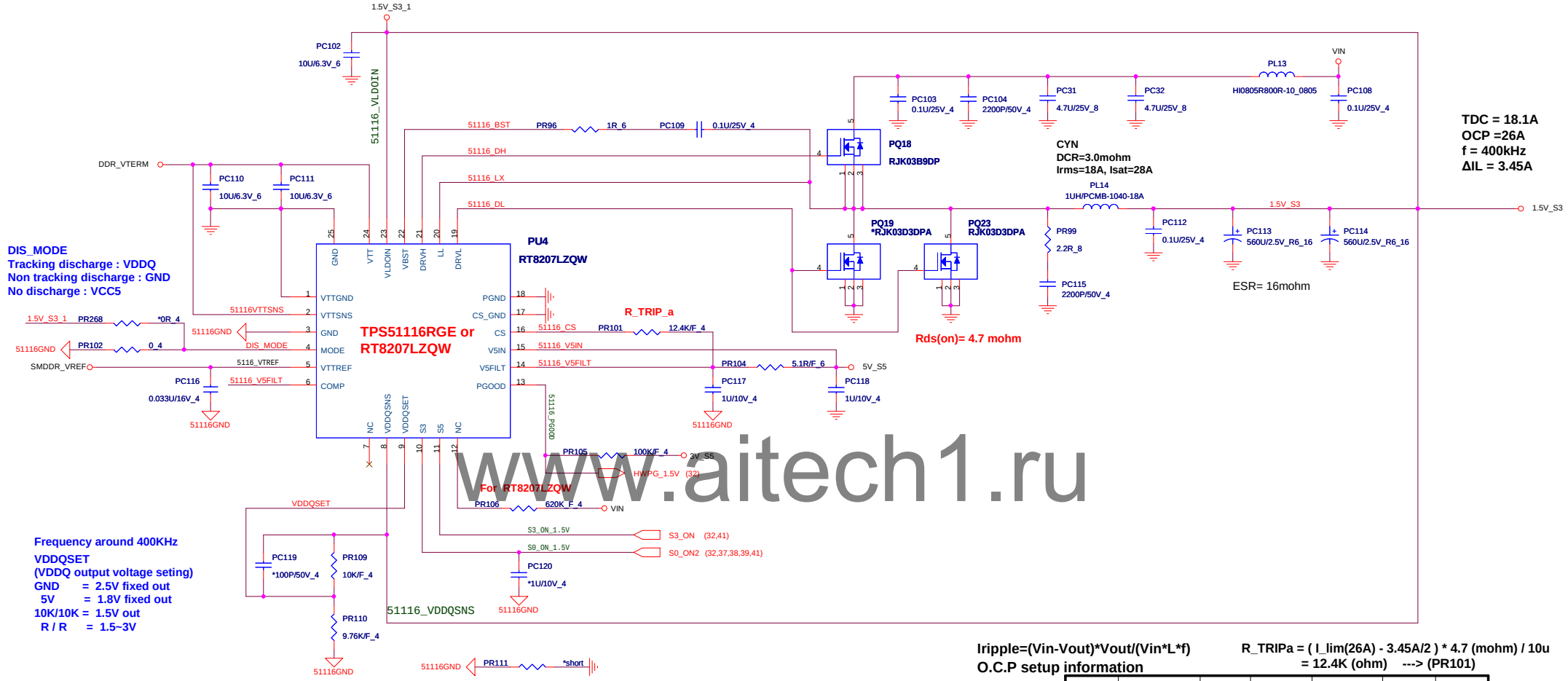
DDR3 1.5V_S3 (TPS51116RGE or RT8207LZQW)



Iripple=(Vin-Vout)*Vout/(Vin*L*f)

R_TRIPa = (I_lim(26A) - 3.45A/2) * 4.7 (mohm) / 10u
= 12.4K (ohm) ---> (PR101)

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
1.5V	4.7m_Max	26	3.45	400	1uH	12.4K

Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size
1uH 20%	CYN	CV-10I0MZ04	18	28	3.3m Max.	11X10X4
1uH 20%	MAG Layer	CV-10L0MZ28	21	30	3.1m Max.	11X10X4

L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
RJK03D3DPA	P_PAK	20A/40A	4.7m	YES
AOL1718	P_PAK	20A/90A	4.3m	YES
RMW200N03FUB	P_PAK	20A/80A	4.6m	NO
FDMS0310S	P_PAK	14A/83A	5.2m	YES

Quanta Computer Inc.
PROJECT : FJ8

Size	Document Number	Rev
	DDR3 1.5V_S3 (RT8207LZQW)	2A

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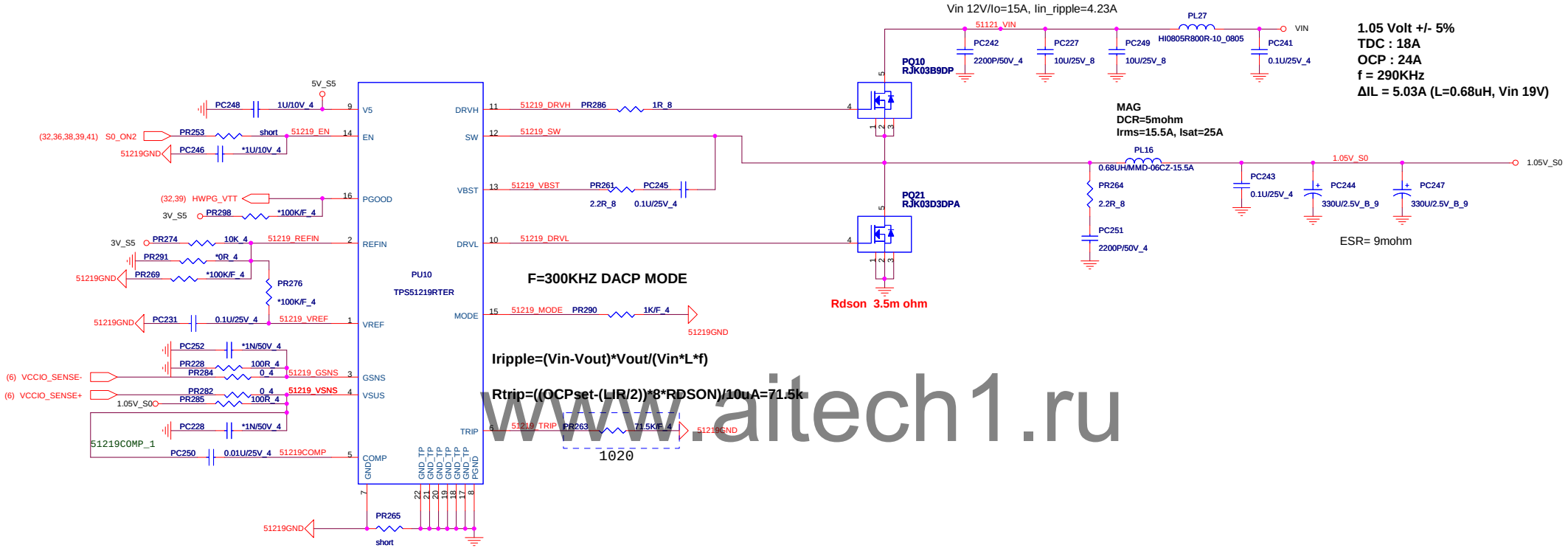
VCCIO and 1.05V_PCH (TPS51219RTER)



VCCIO_SENSE- connect to the GND sense point of the load
VCCIO_SENSE+ connect to the load voltage sense point.

Output Voltage Selection

RFIN=3.3V	output voltage=1.05V
RFIN=GND	output voltage=1.00V
Resister Divider	Adjutable from VREF

Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size
1uH 20%	CYN	CV-10I0MZ04	18	28	3.3m Max.	11X10X4
1uH 20%	MAG Layer	CV-10L0MZ28	21	30	3.1m Max.	11X10X4

O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
1.05V	4.3m_Max	24	3.306	300	1uH	56.2K

Quanta Computer Inc.
PROJECT : FJ8
Size | Document Number: VCCIO and 1.05V_PCH (TPS51219RTER) | Rev 2A
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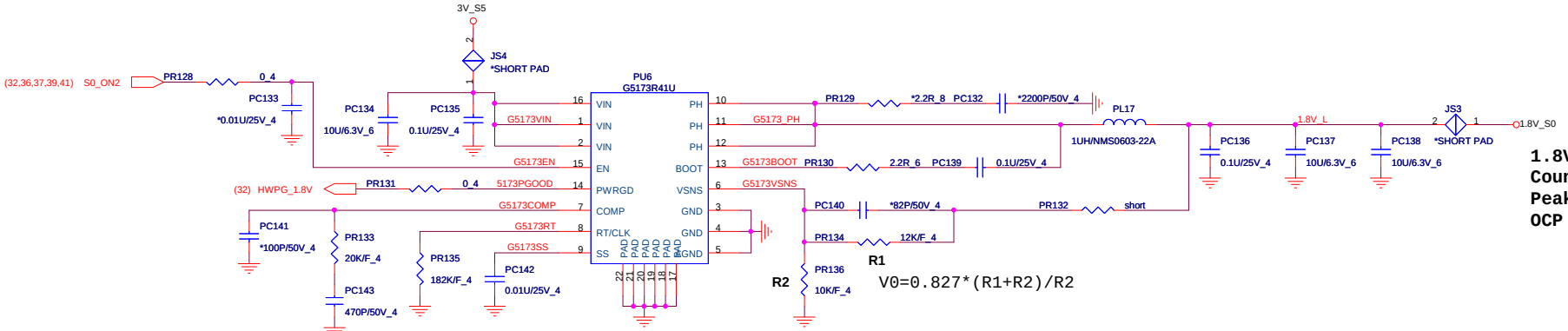
1.8V_S0(G5173R41U)



1.8V_S0 +/- 5%
Countinue current:1.4A
Peak current:3A
OCP minimum 4.5A

Quanta Computer Inc.		
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Size	Document Number: 1.8V_S0(G5173R41U)	Rev: 2A
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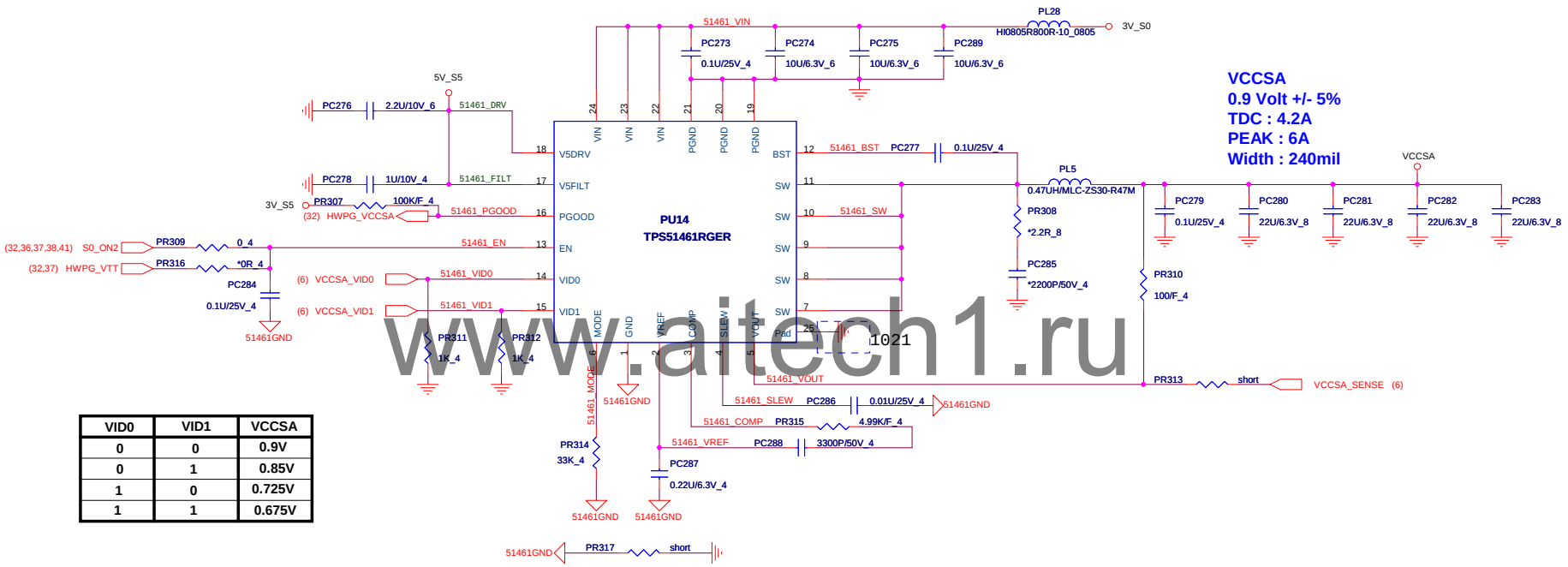
VCCSA (TPS51461RGER)



VID0	VID1	VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.725V
1	1	0.675V

Quanta Computer Inc.
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Size	Document Number	Rev
	VCCSA (TPS51461RGER)	2A

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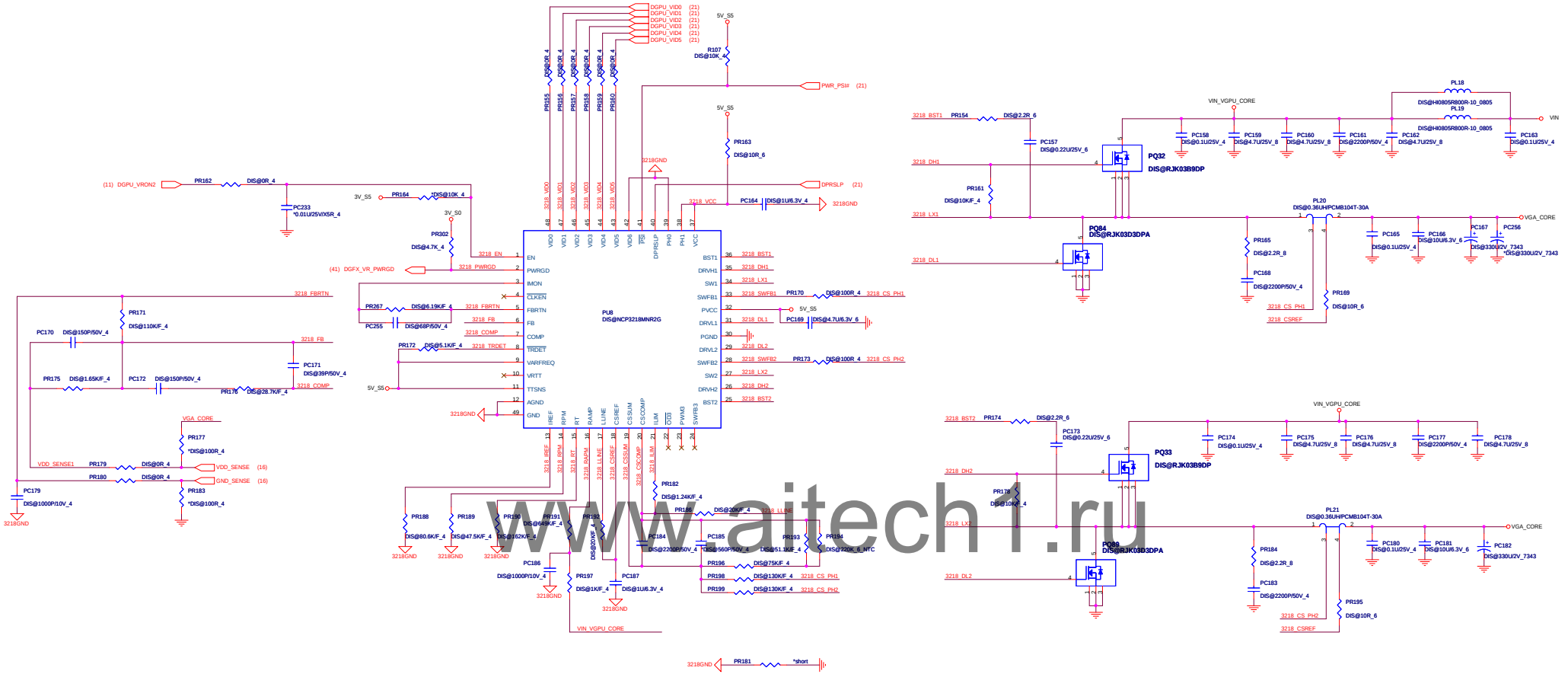

Quanta Computer Inc.		
PROJECT : FJ8		
Size	Document Number	Rev
	VGA_CORE (NCP3218MNR2G)	2A
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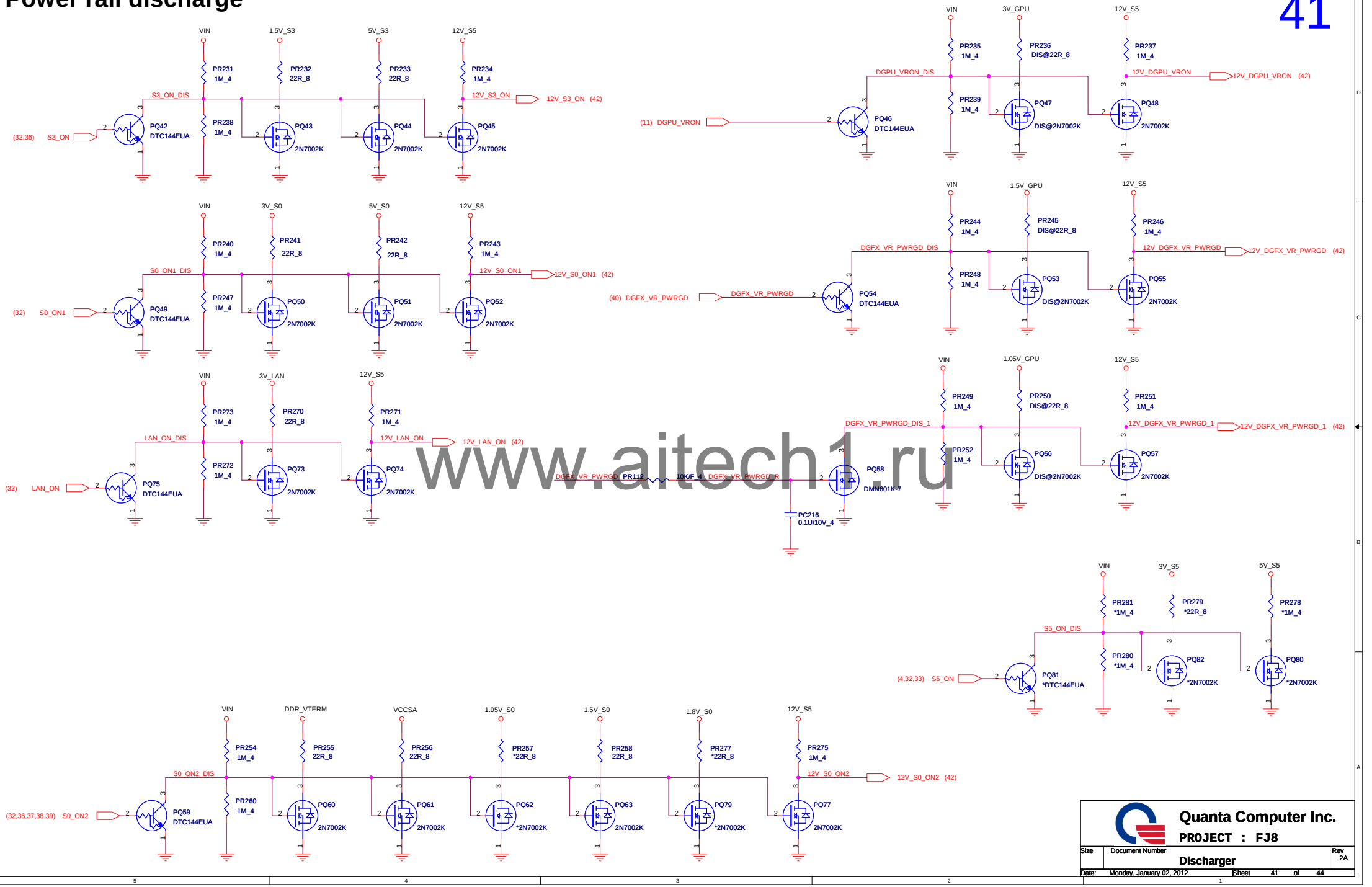
Power rail discharge



Quanta Computer Inc.

PROJECT : FJ8

Size	Document Number	Rev
	Discharger	2A

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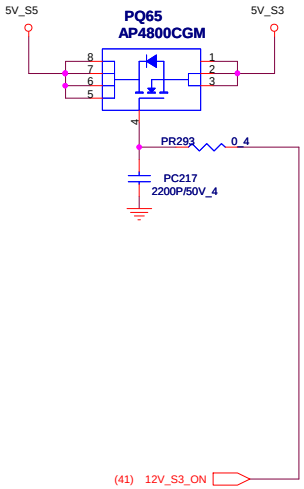
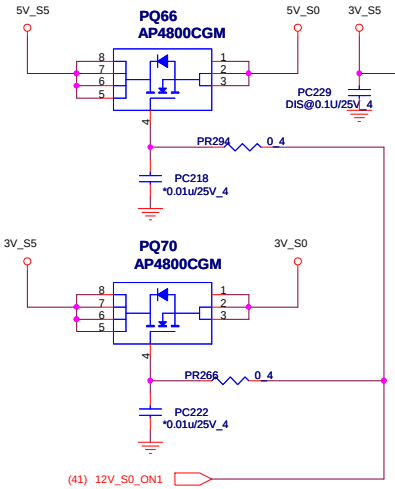
Load Switch

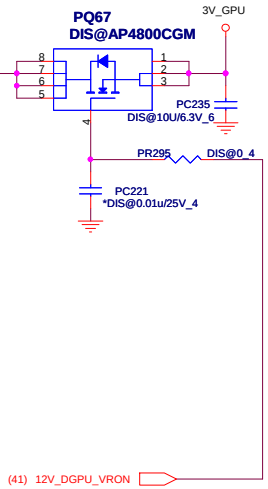
S3 ON Load SW



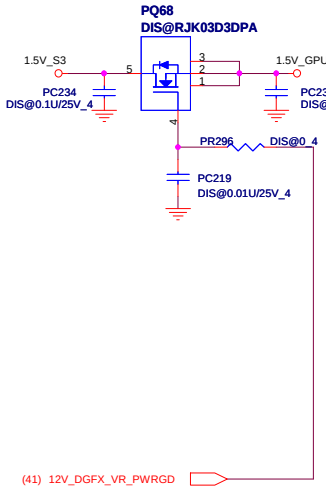
S0 ON1 Load SW



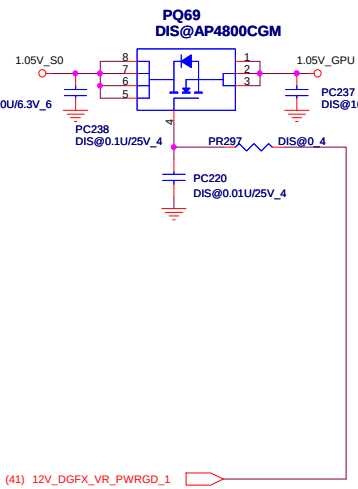
DGPU VRON Load SW



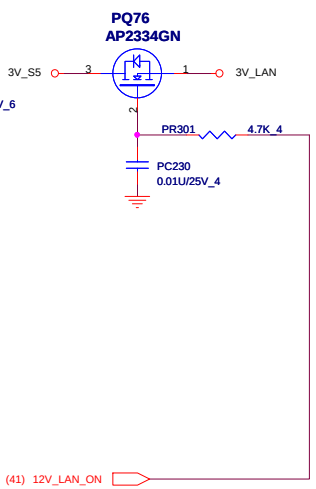
DGFX_VR_PWRGD Load SW



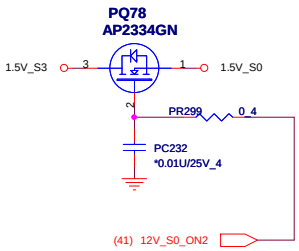
DGFX_VR_PWRGD_1 Load SW



LAN_ON Load SW



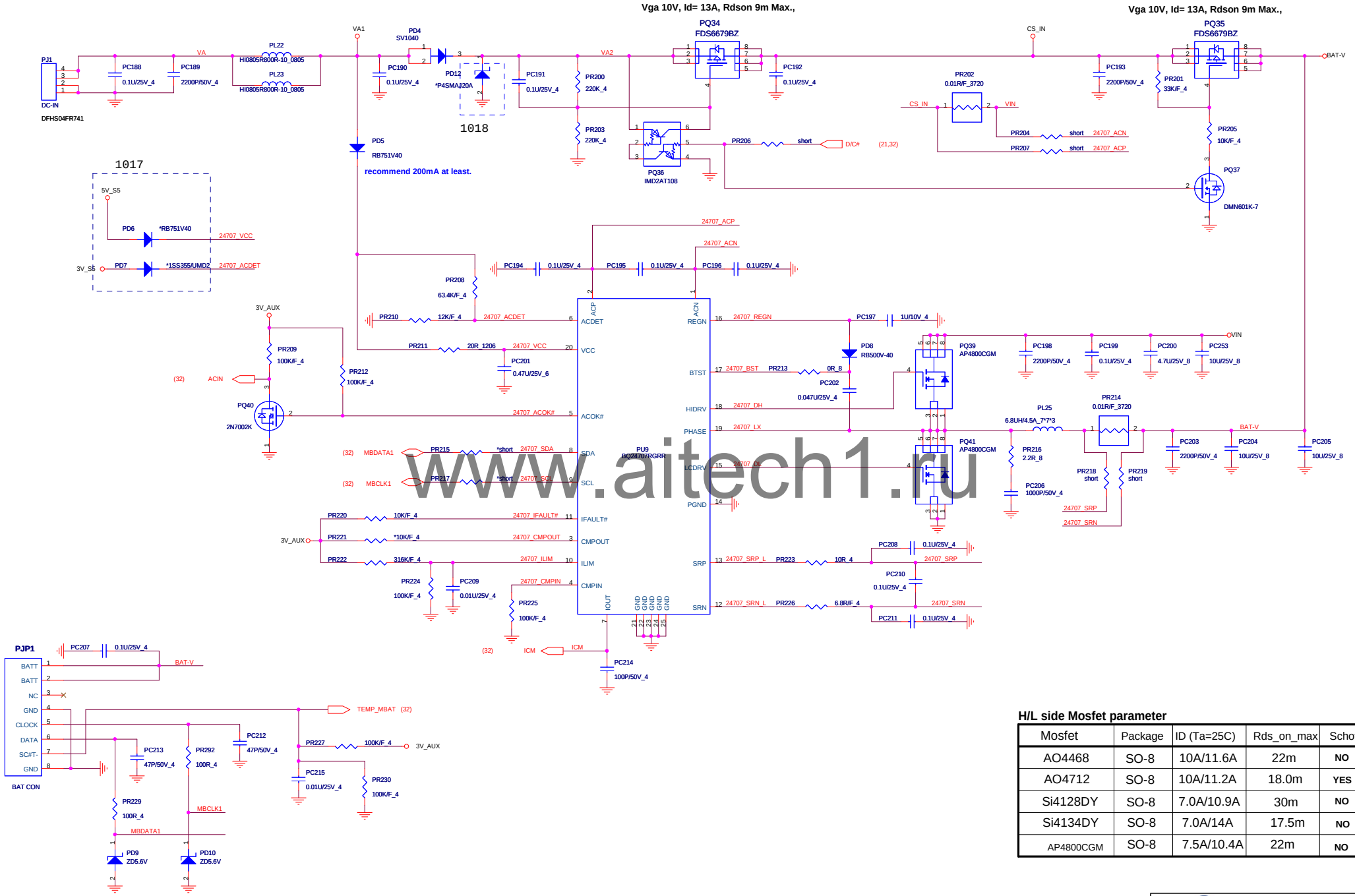
S0 ON2 Load SW



Mosfet parameter

Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
AO4468	SO-8	8.4A/10.4A	22m	+/- 20V
AP4800CGM	SO-8	7.5A/10.4A	22m	+/- 20V
Si4128DY	SO-8	7.0A/10.9A	30m	+/- 20V
Si4134DY	SO-8	7.0A/14A	17.5m	+/- 20V
ME3424D	TSOP-6	5.0A/6.7A	42m	+/- 20V
AP2334GN	SOT-23	4.5A/5.0A	42m	+/- 20V
AO3404	SOT-23	5.0A/5.8A	43m	+/- 20V

Adapter/Battery input & Charger



H/L side Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
AO4468	SO-8	10A/11.6A	22m	NO
AO4712	SO-8	10A/11.2A	18.0m	YES
Si4128DY	SO-8	7.0A/10.9A	30m	NO
Si4134DY	SO-8	7.0A/14A	17.5m	NO
AP4800CGM	SO-8	7.5A/10.4A	22m	NO

Quanta Computer Inc.
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Charger (BQ24707RGRR)
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PCB REV:B

Page 27 : Change CN16,CN18 footprint for smt issue.
Page 27 : Del L20 Add LP19 for EMI issue.
Page 26 : Swap USBP0- & USBP0+ to solve USB can't detect.
Page 21: Add Q41 for correct AC_IN_GPU signal of GPU
Page 32: SWI Add D39 & pull high 10k(R427) to 3V_S5, VRON change to pin107 of EC
Page 27: Add mSATA function of block digarm
Page 17: Modify VL4,VC63,VC64,VC65 from LP@* to DIS@* for provide 1.05V_GPU PLL of VRAM
Page 21: Modify Q36 for discrete mode use and VR53 change to 10K/F_4 from 31K for discrete mode
Page 09,11 : Modify ODD SATA signal from SATA1 to SATA2 of PCH, exchange SATA1GP to SATA2GP
Page 09 : Add U35 4MB ROM for BIOS selection, modify U7 from 8MB ROM to 2MB for ME
Page 09,10,27 : Add SATA signal and repeater for mSATA function, delete 3G_PCIE signal of UMTS
Page 29 : Change Audio codec from Realtek ALC269Q-VC2 to ALC269Q-VC3-GR
Page 40 : Change PR162 from 154kohm to 0ohm for solve leakage current
Page 16 : To match the VY1 frequency stability of oscillation circuit , adjust VC60,VC61 to 27pF from 20pF
Page 16 : For PEX_PLL_HVDD is NC at N13P-GLP GF108, use 0ohm and un-stuff for N13P-GLP to avoid power inrush or leakage to chip internally.
Page 41 : Delete PR300/PD11 and PQ58 change to DMN601K-7 for fix +1.05V_GPU power on sequence.
Page 18 : For GPU debug use, stuff VR31/VR32/VC98 for B stage.
Page 11,32,40: Add U36 & U38 for control GPU power on sequence.
Page 26 : Modify USB S5 charge funtion control signal from EC.
Page 29 : Modify AR13 & AR14 of audio fuction.

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Page 24 : Modify GPIO36_OD_PLG# and GPIO19 strap pin signal design for correct ODD function.
Page 24 : Add D38 for solve HDMI_DDC may enter abnormal when Plug&Play of HDMI.
Page 25 : Change connection around D24 for solve when "5V_CRT2" to GND short, D24 will break at first
Page 25 : Stuff Q21, R332 and un-stuff Q20, R328,R333, R334 for solve DMIC_DAT & CLK signal quality.
Page 27 : ADD R508,R509,R510,Q39,D37 For Win8 wake up function.
Page 09 : For use dual SPI ROM. Change dumping resistor from 0ohm to 33ohm.
Page 27 : Correct for wrong pin connection of mSATA RX pair.
Page 31 : Change con3 footprint.

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Page 25 : Change cn37 footprint to lvds-fi-gr40sb-vf25-dt-40p-l.
Page 10 : Modify SMBUS LEVEL SHIFT circuit for solve leakage current.